





TO-92 Encapsulate Adjustable Reference Source

TL431LK



TO-92 Leaded Plastic Package RoHS compliant

TO-92

FEATURE:

- 1. The output voltage can be adjusted to 40V
- 2. Low dynamic output impedance, its typical value is 0.2Ω
- 3. Trapping current capability is 1 to 100mA
- 4. Low output noise voltage
- 5. Fast on -state response
- 6. The effective temperature compensation in the working range of full temperature
- 7. The typical value of the equivalent temperature factor in the whole temperaturescope is 50 ppm/°C

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Cathode Voltage	V_{KA}	40	V
Cathode Current Range (Continuous)	I _{KA}	-100 to +150	mA
Reference Input Current Range	l _{ref}	0.05 to 10	mA
Power Dissipation	P_{D}	770	mW
Operating Ambient Temperature Range	T_{opr}	-60 to +125	°C
Storage temperature Range	T _{stg}	-60 to +150	°C







ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

DADAMETED	SYMBOL TEST CONDITIONS		VALUE			UNIT	
PARAMETER			MIN	TYP	MAX	UNII	
Reference input voltage (Test ciruit1)	V_{ref}	V _{KA} =V _{REF} , I _{KA} =10mA		2.487	2.5	2.513	V
Deviation of reference input voltage over temperature ¹ (Test ciruit1)	$\Delta V_{ref} / \Delta T$	V _{KA} =V _{REF} , I _{KA} =10mA T _{min} ≤Ta≤T _{max}		I	3	17	mV
Ratio of change in reference input voltage to the change in cathode	$\Delta V_{ref}/\Delta$	l=10mA	$\triangle V_{KA}$ =10V~ V_{REF}		-1.4	-2.7	mV/V
voltage (Test circuit 2)	V_{KA}	I _{KA} - IOIIIA	△V _{KA} =10V~V _{REF} △V _{KA} =36V~ 10V		-1.0	-2.0	μΑ
Reference input current (Test ciruit2)	l _{ref}	I _{KA} = 10mA, R ₁ =10kΩ R2=∞			1.8	4	μΑ
Deviation Of reference input current over full temperature range Test (ciruit2)	$\Delta I_{ref}/\Delta T$	I _{KA} =10mA, R₁=10kΩ R2=∞ Ta=full Temperature range			0.4	1.2	μΑ
Minimum cathode current for regulation (Test ciruit1)	I _{KA(min)}	$V_{KA} = V_{REF}$			0.2	1.0	mA
Off-state cathode Current (Test ciruit3)	I _{KA(OFF)}	V_{KA} =36V, V_{REF} =0			0.05	1.0	μΑ
Dynamic impedance	Z _{KA}	V _{KA} =V _{REF} , f≤1.0kHz I _{KA} =1 to 100mA			0.27	0.45	Ω

Note:

1. T_{MIN} =0°C , T_{MAX} =+70°C



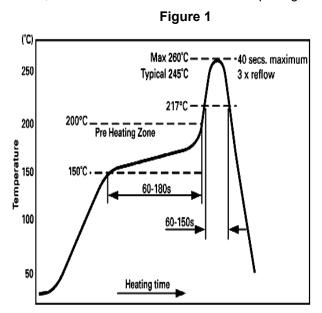


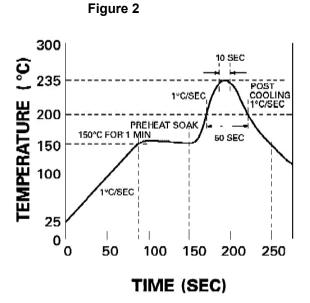
Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.





Reflow profiles in tabular form

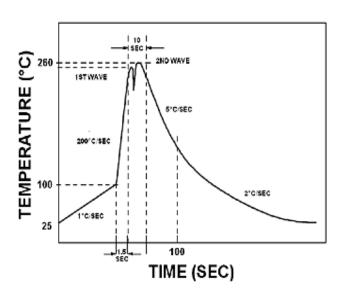
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	150-170°C 60-180 seconds	150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	200°C 30-50 seconds	217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.



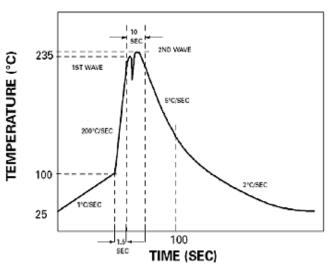


Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

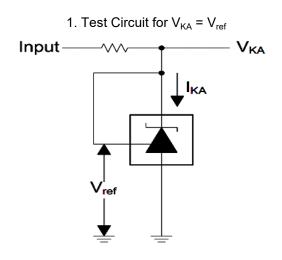
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Vithin 125°C of Solder Tem
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max



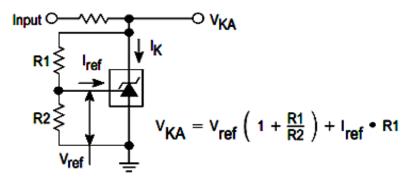




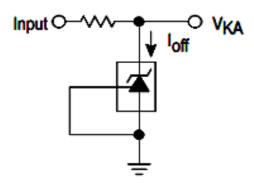
TEST CIRCUIT AND DIAGRAMS



2. Test Circuit for $V_{KA} = V_{ref}$



3. Test Circuit for Ioff







TYPICAL CHARACTERISTICS CURVES

Fig 1: Cathode Current Versus Cathode Voltage

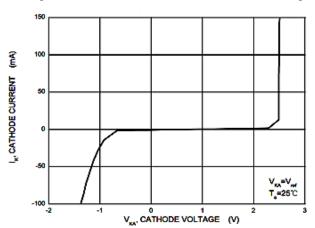


Fig 2: Reference Input Voltage Versus
Ambient Temperature

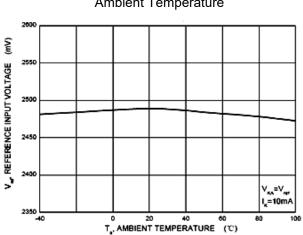


Fig 3: Reference Input Current Versus Ambient Temperature

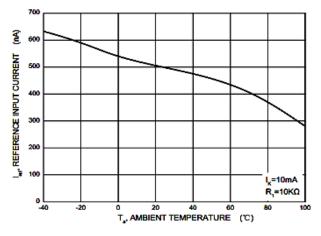


Fig 4: Cathode Current Versus Cathode Voltage

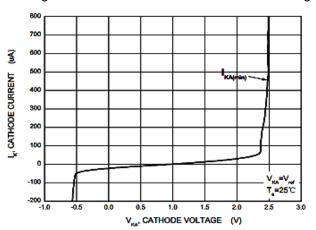


Fig 5: Change in Reference Input Voltage Versus Cathode Voltage

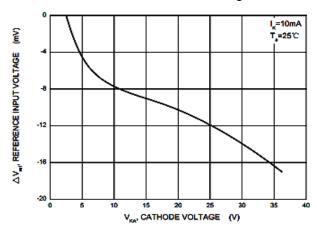
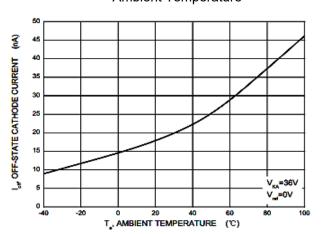


Fig 6: Off-State Cathode Current Versus
Ambient Temperature



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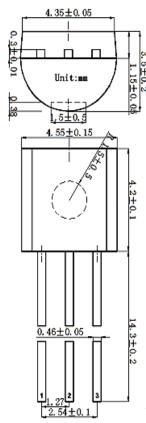






PACKAGE DETAILS

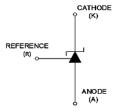
TO-92 Leaded Plastic Package



All Dimensions are in mm

PIN CONFIGURATION

- 1. REFERENCE
- 2. ANODE
- 3. CATHODE







Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- · Temperature 5 °C to 30 °C
- · Humidity between 40 to 70 %RH
- · Air should be clean.
- · Avoid harmful gas or dust.
- · Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- · Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- · Avoid rapid change of temperature.
- · Avoid condensation.
- · Mechanical stress such as vibration and impact shall be avoided.
- · The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level				
Level	Time	Condition		
1	Unlimited	≤30 °C / 85% RH		
2	1 Year	≤30 °C / 60% RH		
2a	4 Weeks	≤30 °C / 60% RH		
3	168 Hours	≤30 °C / 60% RH		
4	72 Hours	≤30 °C / 60% RH		
5	48 Hours	≤30 °C / 60% RH		
5a	24 Hours	≤30 °C / 60% RH		
6	Time on Label(TOL)	≤30 °C / 60% RH		







Customer Notes

Component Disposal Instructions

- 1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
- 2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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