PROGRAMMABLE SHUNT REGULATORS

TL431

TO-92

TO-92
Plastic Package
RoHS compliant

FEATURES:

1. The output voltage can be adjusted to 36V
2. Low dynamic output impedance, it's typical value is 0.2Ω
3. Trapping current capability is 1 to 100mA
4. Low output noise voltage
5. Fast on-state response
6. The effective temperature compensation in the working range of full temperature.
7. The typical value of the equivalent temperature factor in the whole temperature scope is 50ppm/°C

APPLICATIONS:

1. Digital Voltmeters
2. Operational Amplifiers
3. Power Supplies

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Cathode Voltage	V_{KA}	37	V
Cathode Current Range (Continuous)	I_{KA}	-100 to +150	mA
Reference Input Current Range	I_{REF}	0.50 to 10	mA
Power Dissipation	P_D	770	mW
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	162	°C/W
Operating Temperature Range	T_{OPR}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference Input Voltage (Fig. 1)	V_{REF}	$V_{KA}=V_{REF}$, I_{KA}=10mA		2.47	2.50	2.52	V
Deviation of Reference Input Voltage over Temperature (Note) (Fig. 1)	ΔV_{REF} / ΔT	$V_{KA}=V_{REF}$, I_{KA}=10mA $T_{min} \le T_a \le T_{max}$			4.7	17	mV
Ratio of change in reference input voltage to the change in cathode voltage (Fig. 2)	ΔV_{REF} / ΔV_{Ka}	I_{KA} = 10mA	ΔV_{KA}= 10V-V_{REF}		-1	-2.7	mV/V
			ΔV_{KA}= 36V-10V		-0.5	-2	mV/V
Reference Input Current (Fig. 2)	I_{REF}	I_{KA} = 10mA, R1=10KΩ, R2=∞,			1.5	4	µA
Deviation of Reference Input Current over Full Temperature Range (Fig. 2)	ΔI_{REF} / ΔT	I_{KA} = 10mA, R1=10KΩ, R2=∞, T_A= Full Temperature			0.4	1.2	mA
Minimum Cathode Current for Regulation (Fig. 1)	$I_{KA\ (MIN)}$	$V_{KA}=V_{REF}$			0.4	1	mA
Off Stage Cathode Current (Fig. 3)	$I_{KA\ (OFF)}$	V_{KA}=36V, V_{REF}=0			0.05	1	mA
Dynamic Impedance	Z_{KA}	$V_{KA}=V_{REF}$, I_{KA}=1 to 100mA f ≤ 1 KHz			0.15	0.5	Ω

Note:

1. : T_{min} = 0°C, T_{max} = 70°C

CLASSIFICATION OF V_{REF}

Rank	0.50%	1.00%
Range	2.483 ~ 2.507	2.470 ~ 2.520

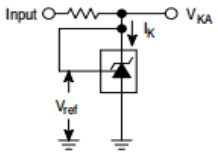


Figure 1. Test Circuit for $V_{KA} = V_{ref}$

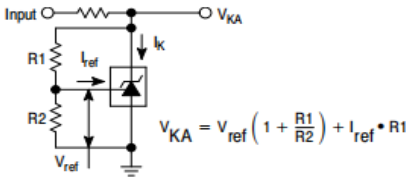


Figure 2. Test Circuit for $V_{KA} > V_{ref}$

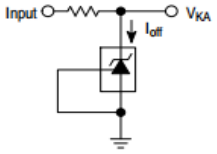


Figure 3. Test Circuit for I_{off}

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

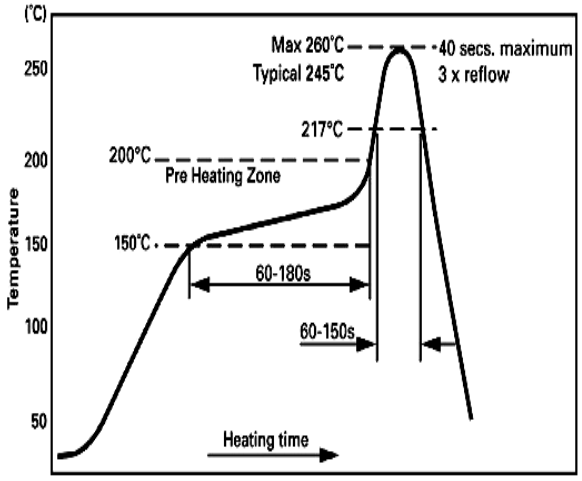
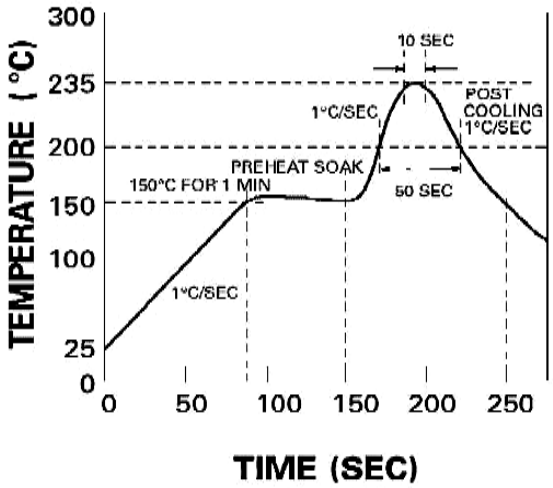


Figure 2

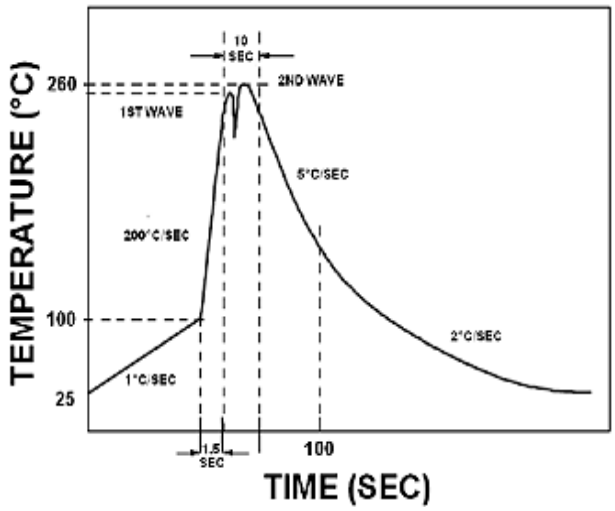


Reflow profiles in tabular form

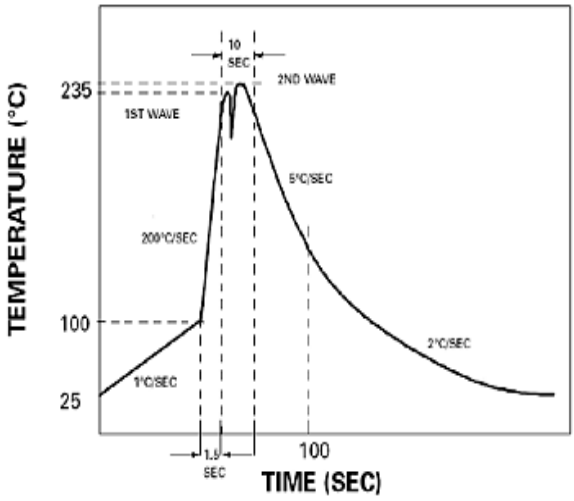
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Typical Characteristic curves

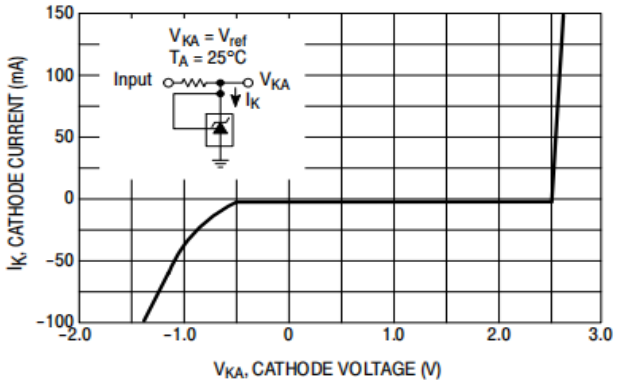


Figure 4. Cathode Current versus Cathode Voltage

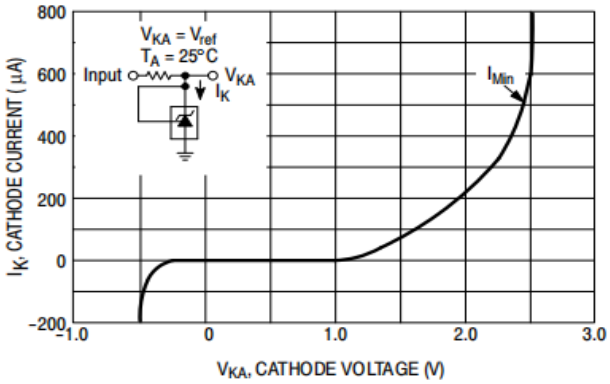


Figure 5. Cathode Current versus Cathode Voltage

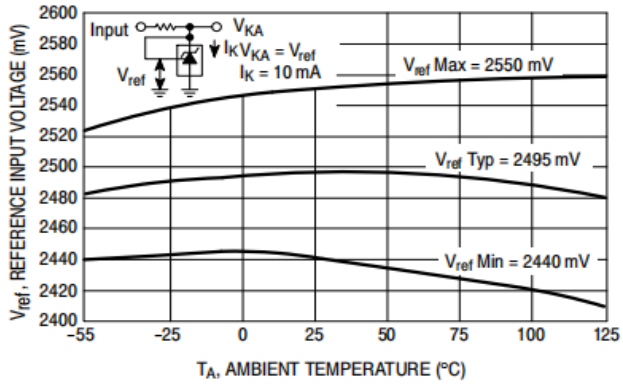


Figure 6. Reference Input Voltage versus Ambient Temperature

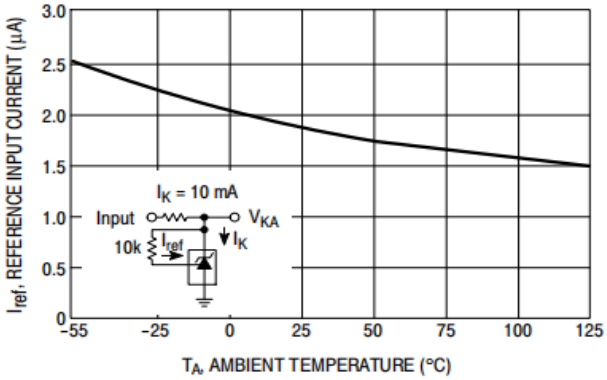


Figure 7. Reference Input Current versus Ambient Temperature

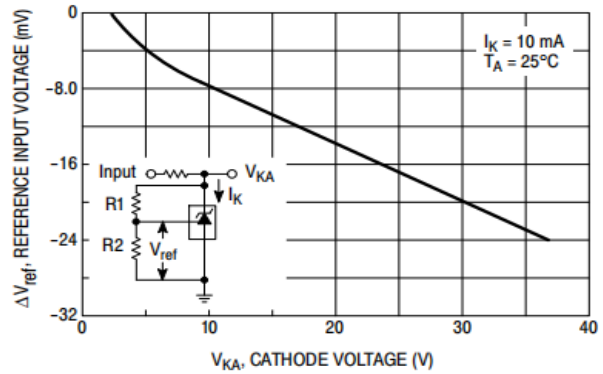


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

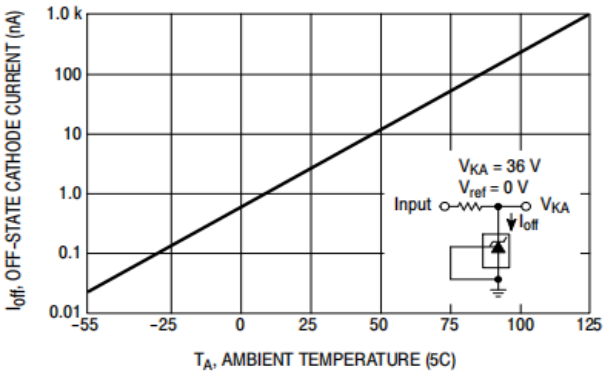


Figure 9. Off−State Cathode Current versus Ambient Temperature

Typical Characteristic curves

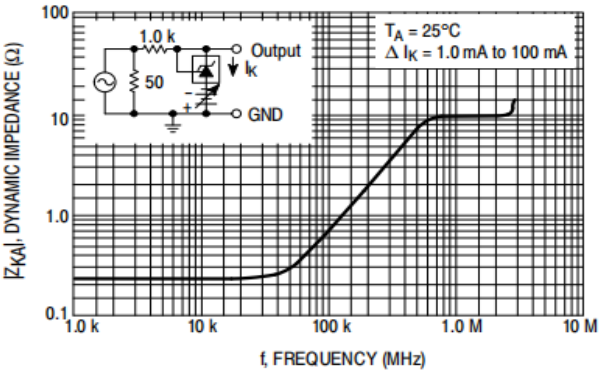


Figure 10. Dynamic Impedance versus Frequency

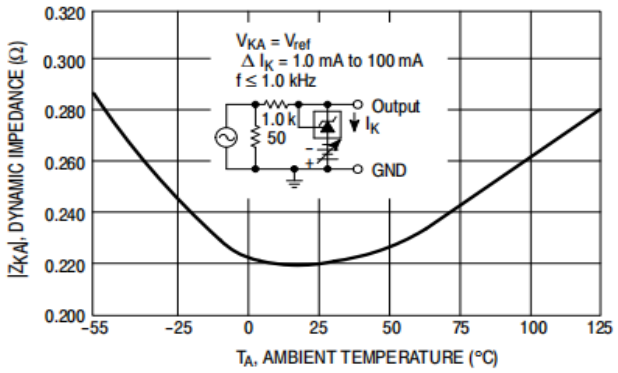


Figure 11. Dynamic Impedance versus Ambient Temperature

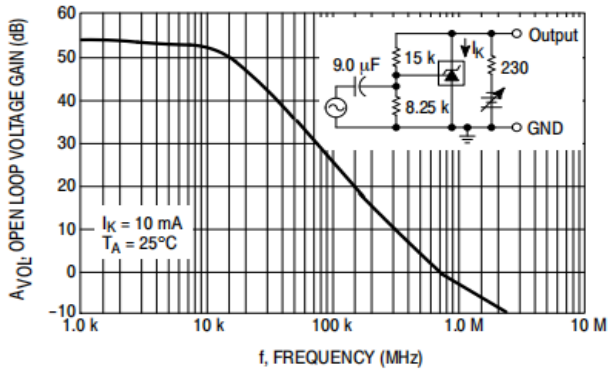


Figure 12. Open−Loop Voltage Gain versus Frequency

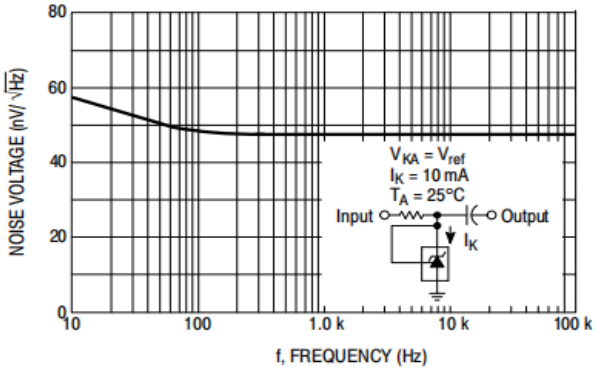


Figure 13. Spectral Noise Density

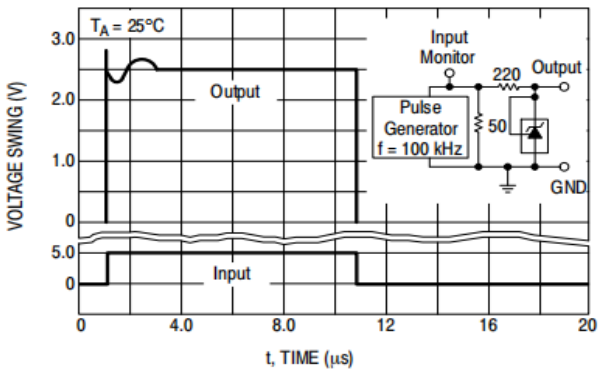
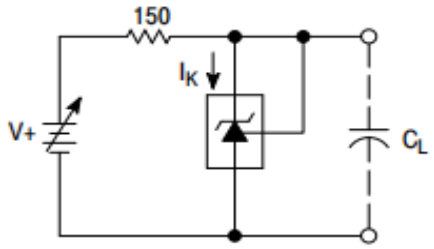


Figure 14. Pulse Response



Test circuit for Figure. 14.

TYPICAL APPLICATIONS

Figure 15. Shunt Regulator

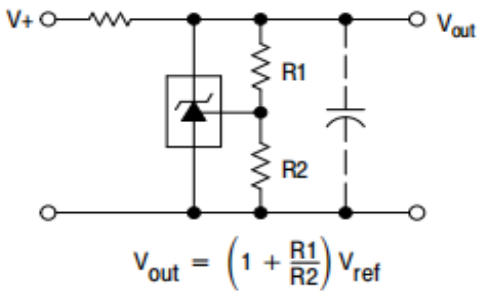


Figure 16. High Current Shunt Regulator

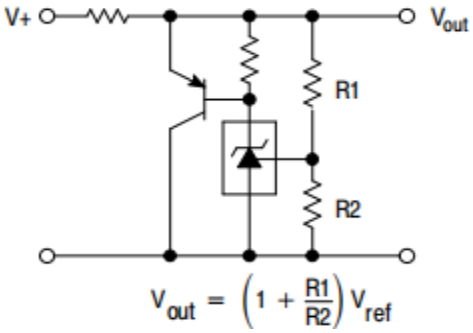


Figure 17. Output Control for a Three−Terminal Fixed Regulator

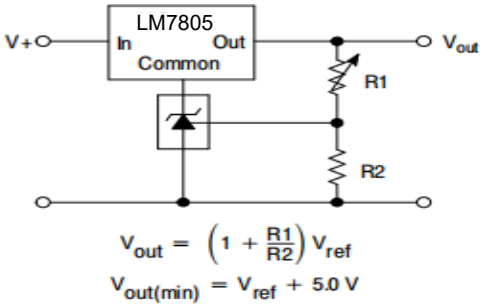


Figure 18. Series Pass Regulator

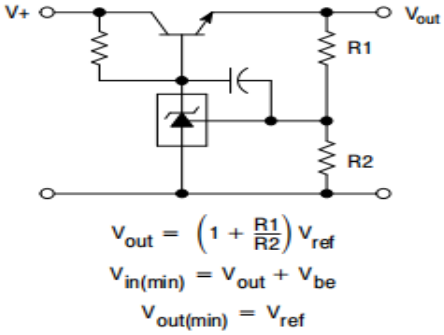


Figure 19. Constant Current Source

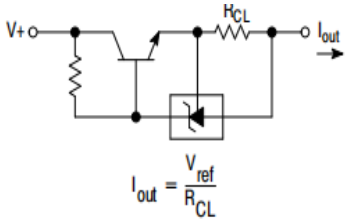


Figure 20. Constant Current Sink

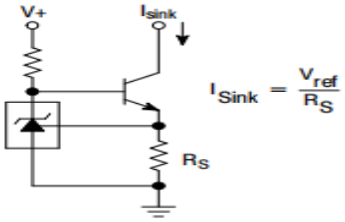


Figure 21. TRIAC Crowbar

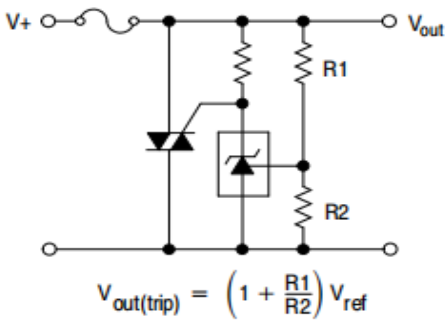
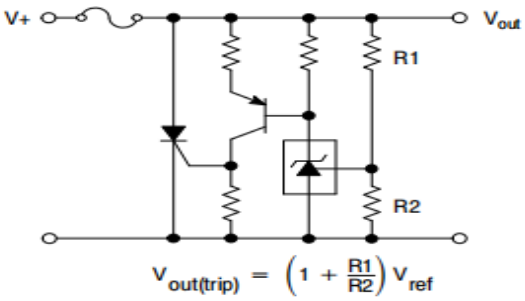
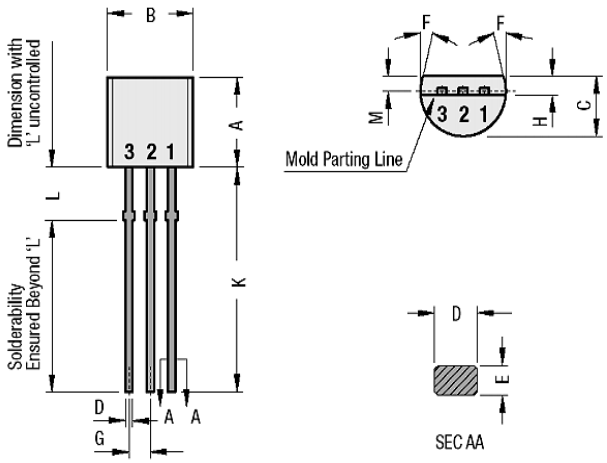


Figure 22. SRC Crowbar



PACKAGE DETAILS

TO-92 Leaded Plastic Package

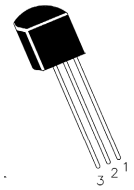


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	
G	1.14	1.40
H	1.20	1.40
K	12.7	
L	1.982	2.082
M	1.03	1.20

All dimensions are in mm

PIN CONFIGURATION

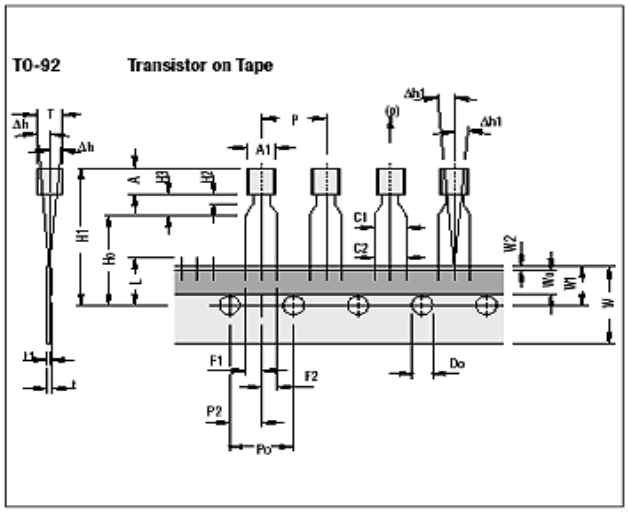
1. Cathode
2. Anode
3. Reference

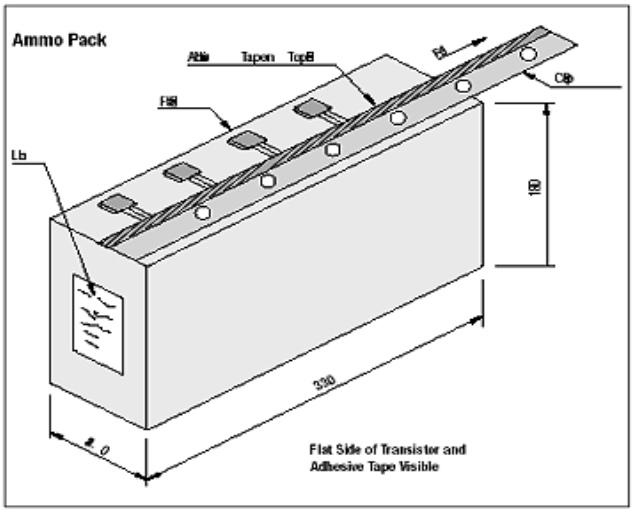


Packaging Information

Package/Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

TO-92 Tape and Ammo Packaging





All Dimensions are in mm

Tape Specifications

		TO-92			
Item description	Symbol	Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[Cr]	P		12.7		±1.0
Feed hole pitch[§1]	Po		12.7		±0.3
Feed hole center to component centre[§2]	P2		6.35		±0.4
Comp. alignment, Side view[§3]	Dh		0	1.0	
Comp. alignment, Front view[§3]	Dh1		0	1.3	
Tape width[Cr]	W		18		±0.5
Hold down tape width[Cr]	Wo		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[Cr]	Do		4		±0.2
Total tape thickness[§4]	t			1.2	
Lead-to-lead distance[Cr]	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelismCr	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 0.6 mm
Cr Critical Dimension.

All Dimensions are in mm

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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