PNP SILICON PLANER EPITAXIAL TRANSISTOR

MPSA92
MPSA93

TO-92

TO-92 Leaded
Plastic Package
RoHS compliant

FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATION:

General Purpose applications, Requiring high Breakdown Voltage, Low Saturation Voltage and low Capacitance.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE		UNIT
			MPSA92	MPSA93	
Collector−Emitter Voltage		V_{CEO}	300	200	V
Collector Base Voltage		V_{CBO}	300	200	V
Emitter Base Voltage		V_{EBO}	5.0		V
Collector Current Continuous		I_C	500		mA
Power Dissipation	T_A = 25°C	P_D	0.625		W
Derate Above 25°C			5.0		mW/°C
Power Dissipation	T_C = 25°C	P_D	1.5		W
Derate Above 25°C			12		mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Junction to Case	$R_{th\ j\text{-}c}$	83.3	°C/W
Junction to Ambient	$R_{th\ j\text{-}a}$	200	°C/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MPSA92		MPSA93		UNIT
			MIN	MAX	MIN	MAX	
Collector Emitter Breakdown Voltage	B_{VCEO} [1]	I_C =1.0mA,I_B = 0	300	--	200	--	V
Collector Base Breakdown Voltage	B_{VCBO}	I_C =100μA,I_E = 0	300	--	200	--	V
Emitter Base Breakdown Voltage	B_{VEBO}	I_E =10μA,I_C = 0	5	--	5.0	--	V
Collector Cut-off Current	I_{CBO}	V_{CB} =160V,I_E=0	--	250	--	250	nA
Emitter Cut-off Current	I_{EBO}	V_{EB} =3.0V, I_C=0	--	100	--	100	nA
DC Current Gain	h_{FE} [1]	I_C=1.0mA, V_{CE}=10V	25	--	25	--	
		I_C=10mA,V_{CE}=10V	40	--	40	--	
		I_C=30mA,V_{CE}=10V	25	--	25	--	
Collector Emitter (Sat) Voltage	$V_{CE(sat)}$ [1]	I_C=20 mA,I_B=2.0mA	--	0.5	--	0.4	V
Base Emitter (Sat) Voltage	$V_{BE(sat)}$ [1]	I_C=20 mA,I_B=2.0mA	--	0.9	--	0.9	V
DYNAMIC CHARACTERISTICS							
Current Gain-Bandwidth Product	f_T	I_C=10mA,V_{CE}=20V, f =100MHz	50	--	50	--	MHz
Collector Base Capacitance	C_{cb}	V_{CB}=20V,I_E=0,f =1.0MHz	--	6.0		8.0	pF

Note:

1. Pulse Test: Pulse Width ≤=300 μs, Duty Cycle ≤= 2%.

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

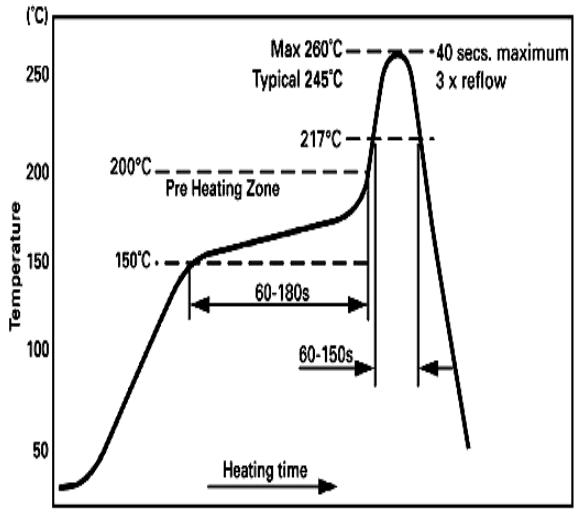
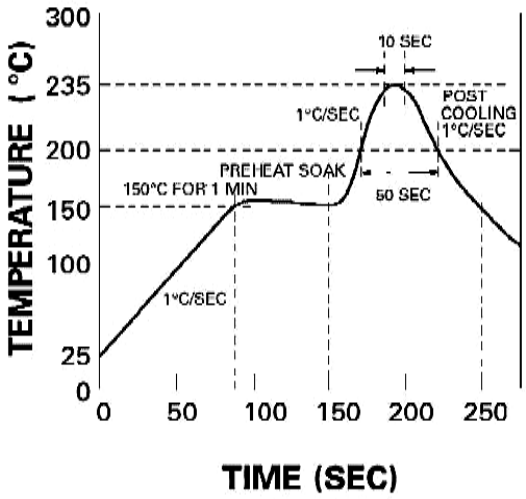


Figure 2

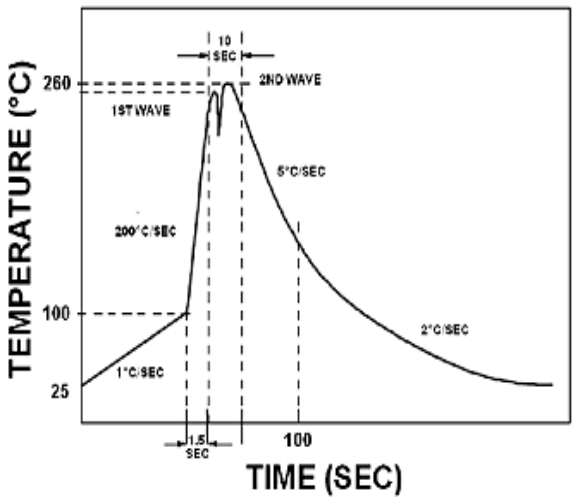


Reflow profiles in tabular form

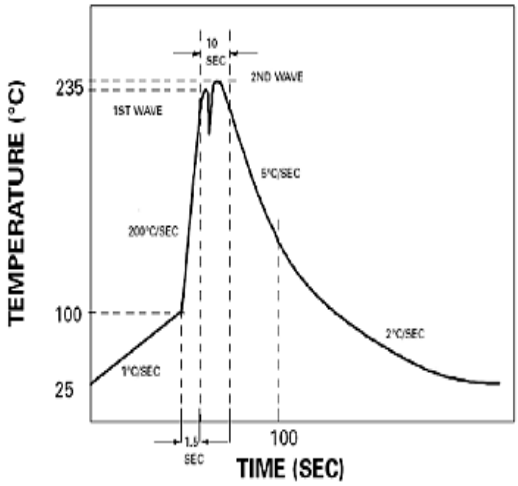
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat		
Time maintained above:		
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: DC Current Gain

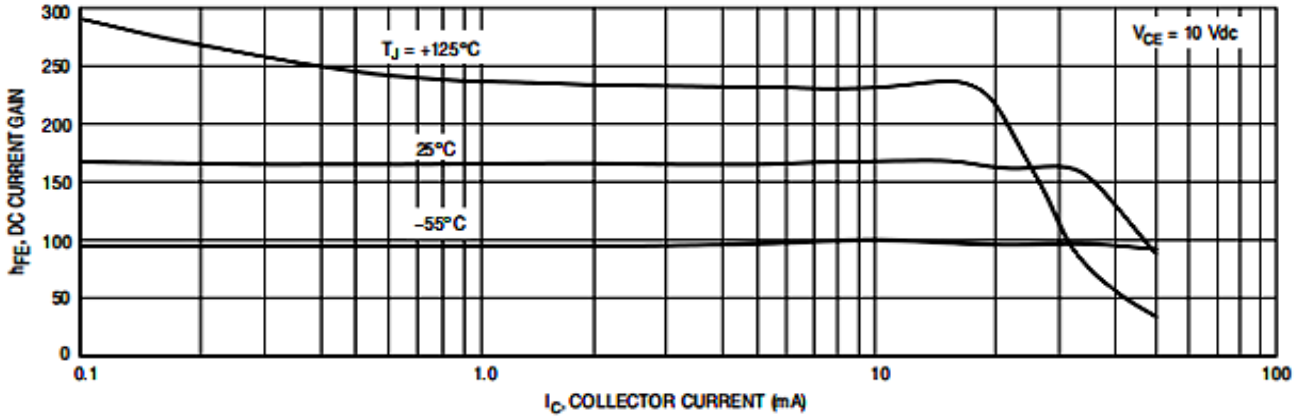


Fig 2: Capacitance

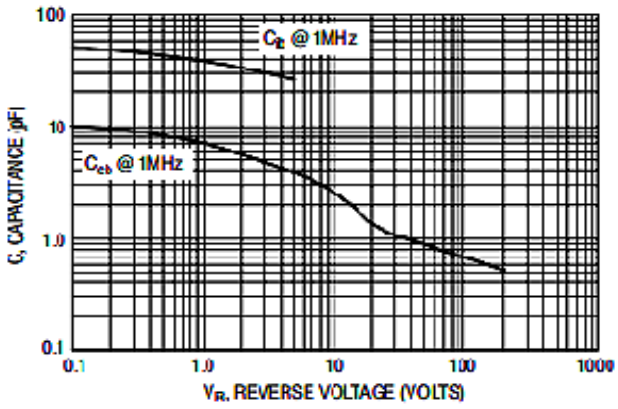


Fig 3: ”ON” Voltages

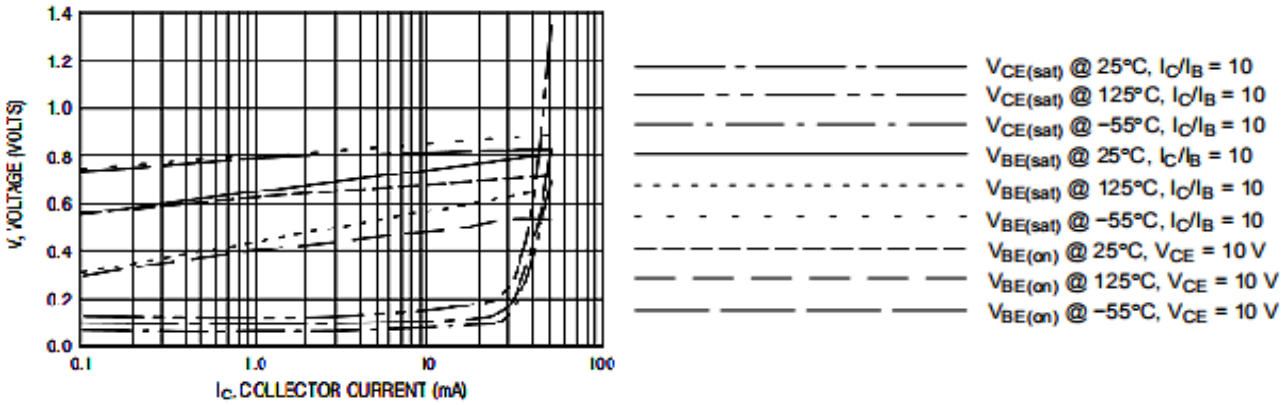
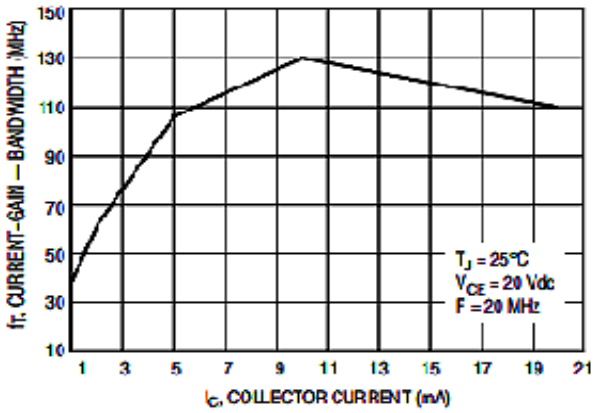
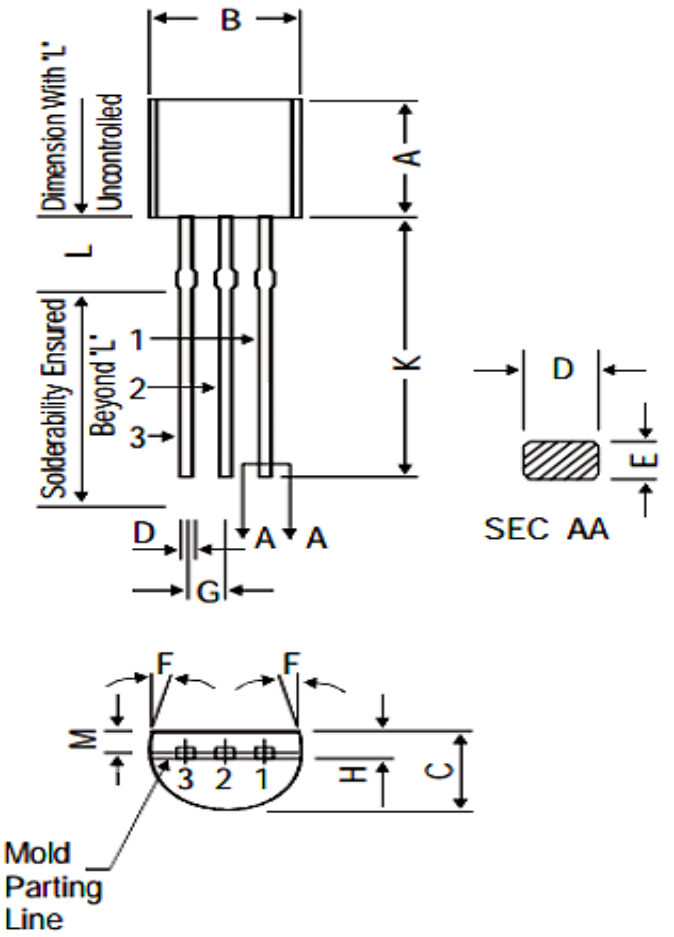


Fig 4: Current−Gain − Bandwidth



PACKAGE DETAIL

TO-92 Leaded Plastic Package

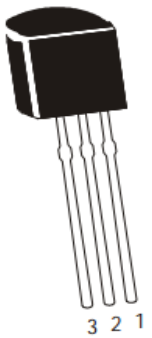


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5 DEG	
G	1.14	1.40
H	1.20	1.40
K	12.7	--
L	1.98	2.08
M	1.03	1.20

All Dimensions are in

PIN CONFIGURATION

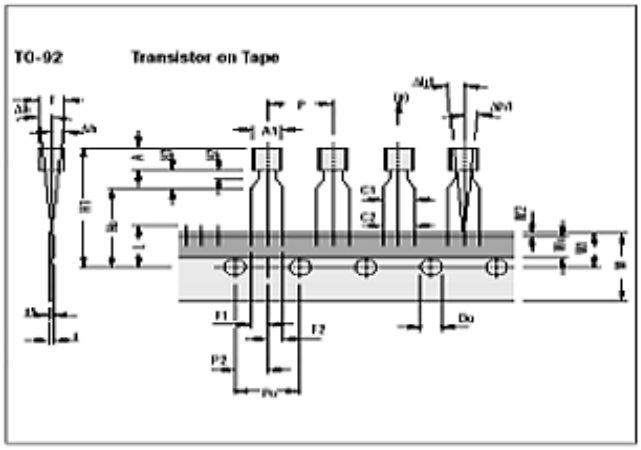
1. COLLECTOR
2. BASE
3. EMITTER

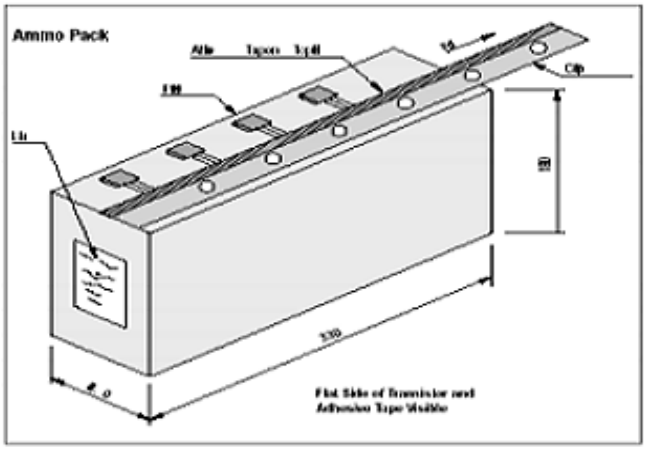


Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5K	17" x 15" x 13.5"	80K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2K	17" x 15" x 13.5"	32K	12.5 kgs

TO-92 Tape and Ammo Pack





All dimensions are in mm

ITEM	SYMBOL	SPECIFICATION			
		MIN.	NOM.	MAX.	TOL.
BODY WIDTH	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[cr]	P		12.7		±1.0
Feed hole pitch[51]	Po		12.7		±0.3
Feed hole centre to component centre[52]	P2		6.35		±0.4
Comp. alignment,side view[53]	Dh		0	1.0	
Comp. alignment,front view [53]	Dh1		0	1.3	
Tape width[cr]	W		18		±0.5
Hole-down tape width[cr]	Wo		6		±0.2
Hole position	W1		9		±0.7-0.5
Hole-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[cr]	Do		4		±0.2
Total tape thickness[54]	t			1.2	
Lead-to-lead distance[cr]	F1,F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelism[cr]	C1-C2			0.22	
pull-out force	(p)	6N			

Note:

1. Maximum alignment deviation between leads not to be greater BODY W then 0.20 mm.
2. Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
3. Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive
4. No more then 3 consecutive missing components is permitted
5. A tape trailer, having at least three feed holes is required after Ho the last component
6. Splices shall not interfere with the sprocket feed holes

*1 Cumulative pitch error 1.0 mm/20 pitch.

*2. To be measured at bottom of clinch.

*3. At top of body.

*4. t1=0.3-0.6 mm

*5. Critical Dimension.

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Rev0 23122020EM

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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