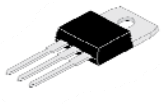
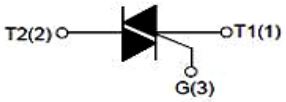
4A TRIACs

CST04-1000SW



TO-220B



TO-220B
Non- Insulated
Plastic Package
RoHS compliant

GENERAL DISCRIPTION:

With high ability to withstand the shock loading of large current, CST04-1000SW series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, the products especially recommended for use on inductive load.From all three terminals to external heatsink, CST04-1000SW provides a rated insulation voltage of 2500 VRMS, The package is RoHS compliant. (2011/65/EU)

FEATURE:

PARAMETER	SYMBOL	VALUE	UNIT
RMS on-state current	$I_{T(RMS)}$	4	A
Non repetitive surge peak Off-state voltage/ Repetitive peak reverse voltage(Tj=25℃)	V_{DRM} /V_{RRM}	1000	V

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		T_{stg}	-40 to +150	°C
Operating junction temperature range		T_j	-40 to +125	°C
Repetitive peak off-state voltage(T_j=25°C)		V_{DRM}	1000	V
Repetitive peak reverse voltage(T_j=25°C)		V_{RRM}	1000	V
RMS on-state current	TO-220B	$I_{T(RMS)}$	4	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	40	A
I^2t value for fusing (tp=10ms)		I^2t	8	A^2s
Critical rate of rise of on-statecurrent (I_G=2×I_{GT})		dI/dt	50	A/μs
Peak gate current		I_{GM}	4	A
Average gate power dissipation		$P_{G(AV)}$	1	W
Peak gate power dissipation		P_{GM}	5	W

THERMAL RESISTANCES

PARAMETER	SYMBOL	TEST CONDITION	VALUE	UNIT
Junction to case thermal resistance	$R_{th(j-c)}$	Junction to case(AC)	2.5	°C/W

CST04-1000SW
Rev03 22062022EBJ

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	Quadrant	TEST CONDITION	VALUE			UNIT
				MIN	TYP	MAX	
Triggering gate current	$I_{GT\ (Max)}$	**I-II-III**	V_D=12V R_L=33Ω	--	--	10	mA
Triggering gate voltage	$V_{GT\ (Max)}$	**I-II-III**		--	--	1.5	V
Non-triggering gate voltage	$V_{GD\ (Min)}$	**I-II-III**	V_D=V_{DRM} T_j=125°C, R_L=3.3KΩ	--	--	0.2	V
Latching current	$I_{L\ (Max)}$	**I-III**	I_G=1.2I_{GT}	--	--	20	mA
		II		--	--	35	
Holding current	$I_{H\ (Max)}$	**ALL**	I_T=100mA	--	--	15	mA
Critical rate of rise of off-state voltage	dV/dt (Min)	V_D=2/3V_{DRM} Gate Open T_j=125°C		--	--	100	V/μs
STATIC CHARACTERISTICS							
Peak on-state voltage drop	V_{TM}	Tj=25°C	I_{TM} =5.5A t_p=380μs	--	--	1.5	V
Max. Forward Current	I_{DRM}	Tj=25°C	V_D=V_{DRM} V_R=V_{RRM}	--	--	10	μA
Max. Reverse Current	I_{RRM}	Tj=125°C		--	--	0.75	mA

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

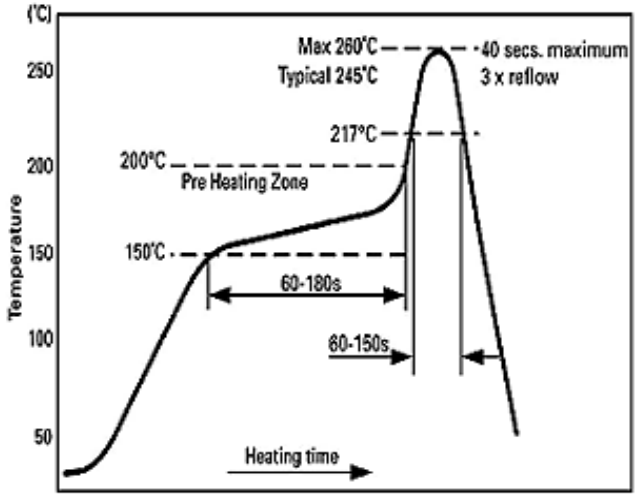
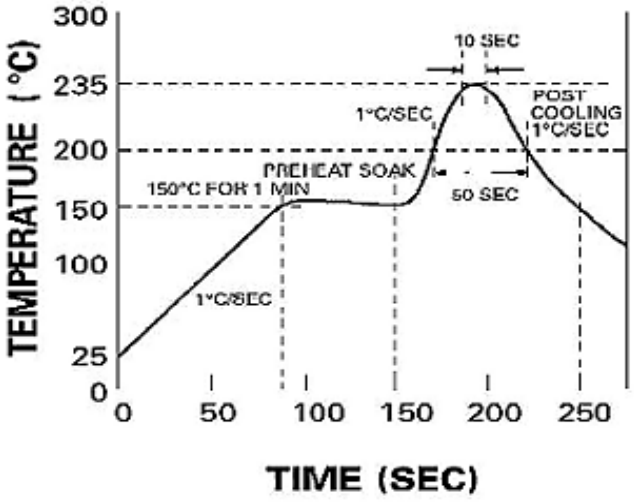


Figure 2

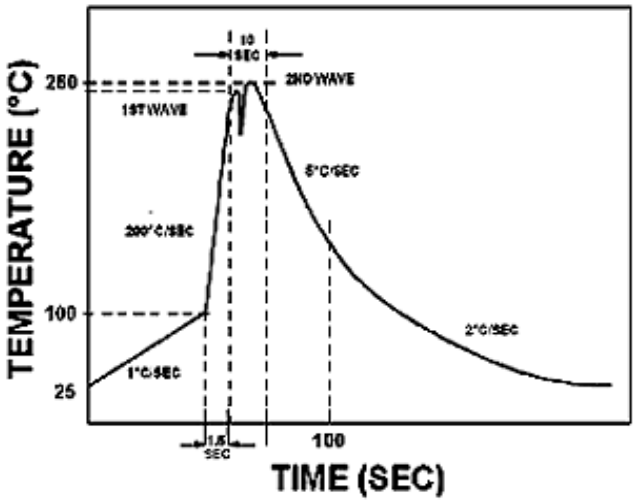


Reflow profiles in tabular form

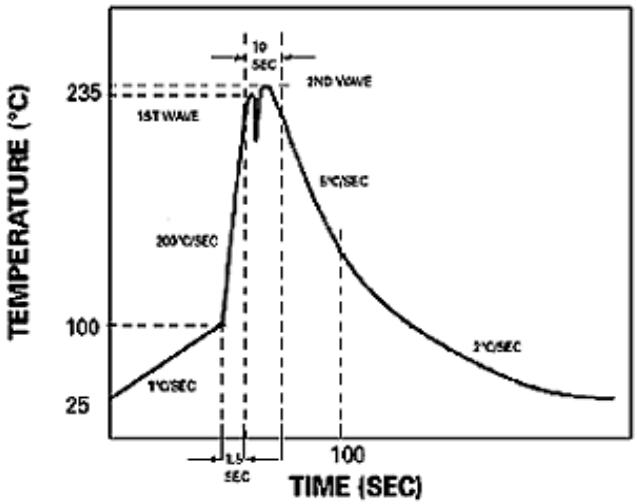
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Tim	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum Power Dissipation Versus RMS case Temperature

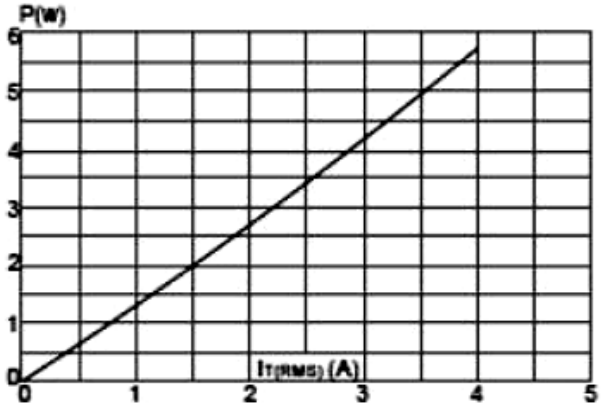


Fig 2: Surge peak On-state Current Versus number of Cycles

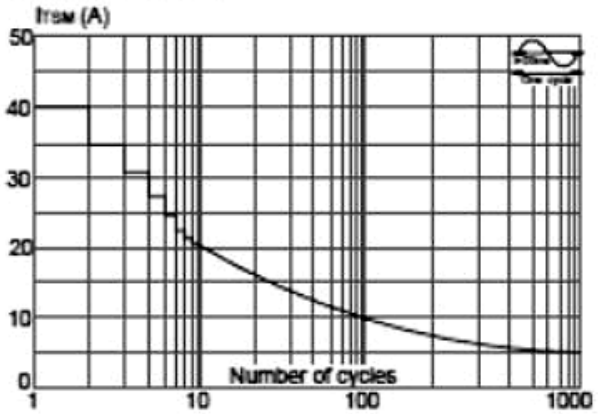


Fig 3: Non-Repetitive Surge peak on-state current for a sinusoidal pulse with width tp < 20ms and corresponding value of I2t(dl/dt<50A/µs)

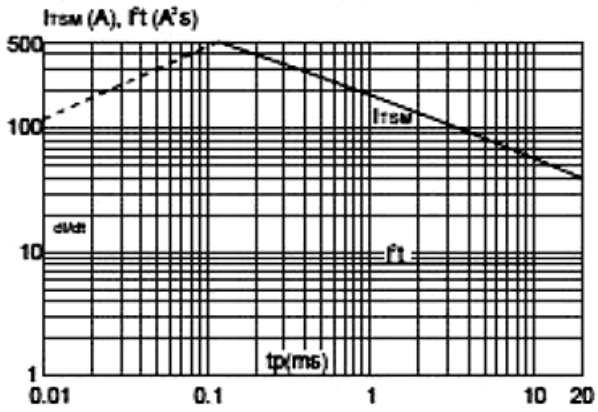


Fig 4: RMS On-state Current Versus case Temperature

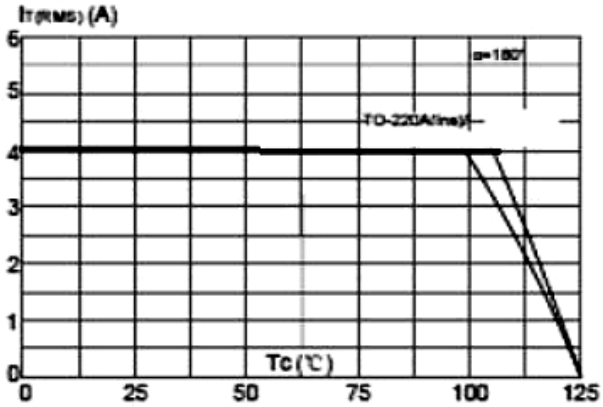


Fig 5: On-State Characteristics (Maximum Values)

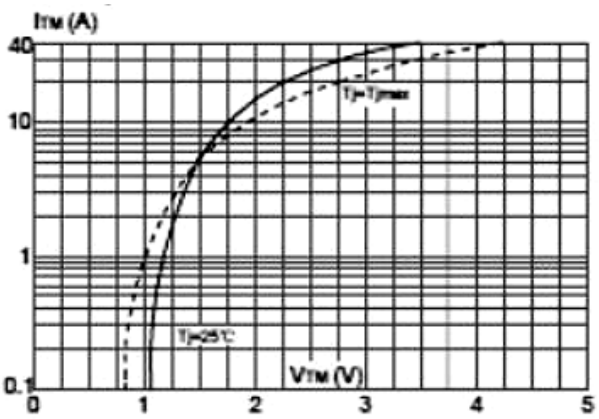
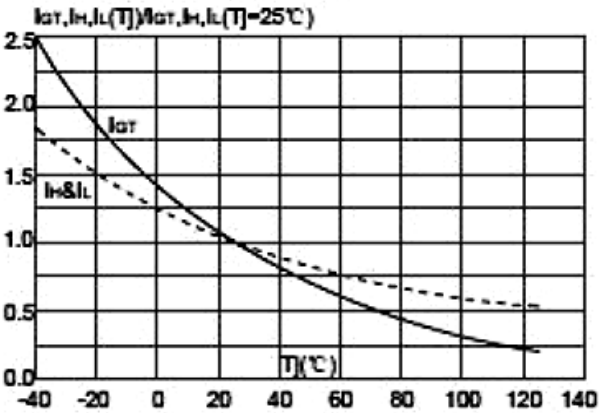
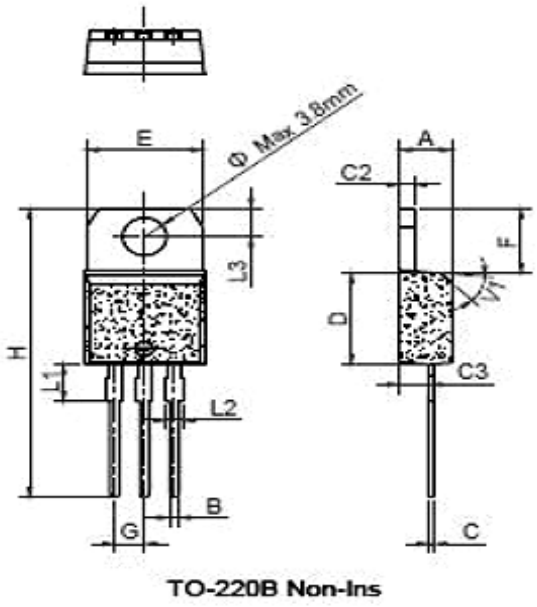


Fig 6: Relatitive variations of gate trigger current holding current and latching current versus junction temperature



PACKAGE DETAILS

TO-220B Non-Ins Plastic Package



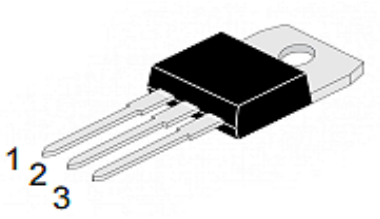
TO-220B Non-Ins

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	0.61		0.88	0.024		0.035
C	0.46		0.70	0.018		0.028
C2	1.21		1.32	0.048		0.052
C3	2.40		2.72	0.094		0.107
D	8.60		9.70	0.339		0.382
E	9.60		10.4	0.378		0.409
F	6.20		6.60	0.244		0.260
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.75			0.148	
L2	1.14		1.70	0.045		0.067
L3	2.65		2.95	0.104		0.116
V1		45°			45°	

All Dimensions are in mm

Pin Confoguration

1. T1
2. T2
3. G



Packing Details

PACKAGE	OUTLINE	TUBE (Pcs)	INNER BOX (Pcs)	PER CARTOON
TO-220B	TUBE	50	1000	8000

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving /support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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