EPITAXIAL TRANSISTORS

NPN PNP
CNL635 CPL636
CNL637 CPL638
CNL639 CPL640

TO-92

TO-92
Plastic Package
RoHS compliant

FEATURE:

1. This product is available in AEC-Q101 Qualified and PPAP Capable also.

Note: For AEC-Q101 qualified products, please use suffix -AQ in the part number while ordering.

APPLICATIONS:

Complementary Silicon Transistors For Switching And Linear Applications DC Amplifier & Driver For Industrial Applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	CNL635 CPL636	CNL637 CPL638	CNL639 CPL640	UNIT
Collector Emitter Voltage	V_{CEO}	45	60	80	V
Collector Base Voltage	V_{CBO}	45	60	80	V
Emitter Base Voltage	V_{EBO}	5			V
Collector Current Continuous	I_C	1			A
Collector Current Peak	I_{CM}	1.5			A
Base Current Continuous	I_B	100			mA
Base Current Peak	I_{BM}	200			mA
Power Dissipation @ Ta=25ºC	P_D	0.8			W
Power Dissipation @ Ta=25ºC	P_D [1]	1.0			W
Power Dissipation @ Tc=25ºC	P_D	2.0			W
Operating And Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150			°C

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	Part no.	VALUE MAX	VALUE MIN	UNIT
Collector Emitter Voltage	V_{CEO}	I_C=1mA, I_B=0	CNL635,CPL636	45	--	V
			CNL637,CPL638	60	--	
			CNL639,CPL640	80	--	
Collector Base Voltage	V_{CBO}	I_C=100m A, I_E=0	CNL635,CPL636	45	--	V
			CNL637,CPL638	60	--	
			CNL639,CPL640	100	--	
Emitter Base Voltage	V_{EBO}	I_E=10m A, I_C=0		5	--	V

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	VALUE		UNIT
				MAX	MIN	
Collector Cut-off Current		I_{CBO}	V_{CB}=30V, I_E = 0	--	100	nA
			V_{CB}=30V, I_E = 0, T_a=125°C	--	10	μA
Base Emitter On Voltage		$V_{BE(on)}$ [2]	V_{CE}=2V, I_C = 500mA	--	1	V
Collector Emitter Saturation Voltage		$V_{CE(sat)}$ [2]	I_C=500mA, I_B=50mA	--	0.5	V
DC Current Gain		h_{FE} [2]	V_{CE}=2V, I_C=5mA	25	--	
			V_{CE}=2V, I_C=150mA	40 ~ 250		
			V_{CE}=2V, I_C=500mA	25	--	
Input Capacitance	NPN	C_{ib}	V_{BE}=0.5V, I_C=0, f=1MHz	50 TYP		pF
	PNP			110 TYP		pF
Output Capacitance	NPN	C_{ob}	V_{CB}=10V, I_C=0, f=1MHz	7 TYP		pF
	PNP			9 TYP		pF
Transition Frequency	NPN	f_T	I_C=50mA, V_{CE}=2V, f=100MHz	200 TYP		MHz
	PNP			150 TYP		MHz

Note:

1. Transistors mounted on printed circuit board. Lead Length 4mm, mounting pad for collector lead min
2. Pulse Test: Pulse Width ≤ 300ms; Duty Cycle ≤ 2%
3. For PNP device voltage and current values will be negative (-).

Typical Characteristic curves

Fig. 1. Total power dissipation Ptot = f (TA; TC)

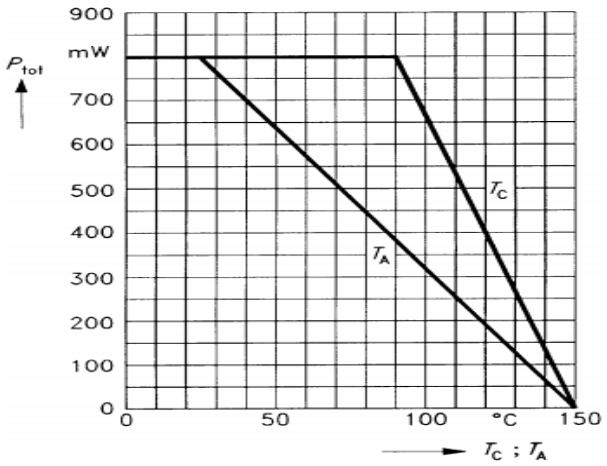


Fig. 4. Collector current IC = f (VBE)

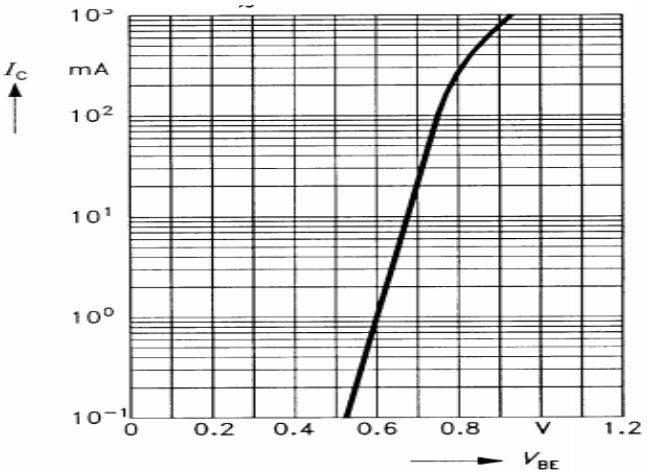


Fig.2. Permissible pulse load RthJA = f (tp) VCE = 2 V

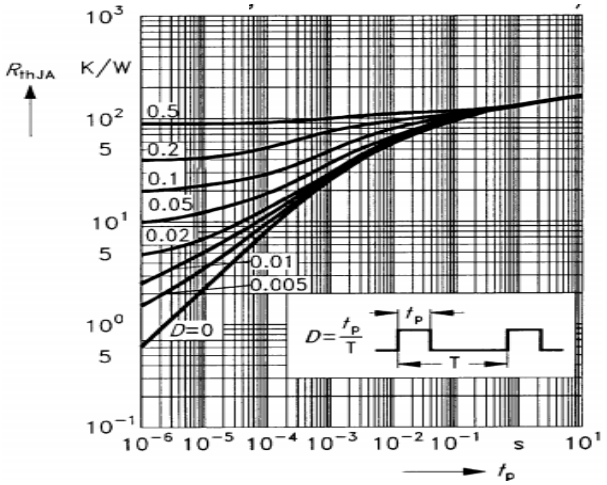


Fig. 5. DC current gain hFE = f (IC) VCE = 2 V

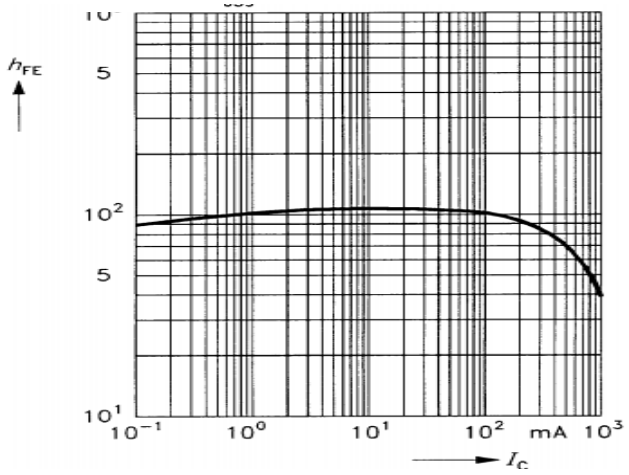


Fig.3. Collector cutoff current ICB0 = f (TA) VCB = 30 V

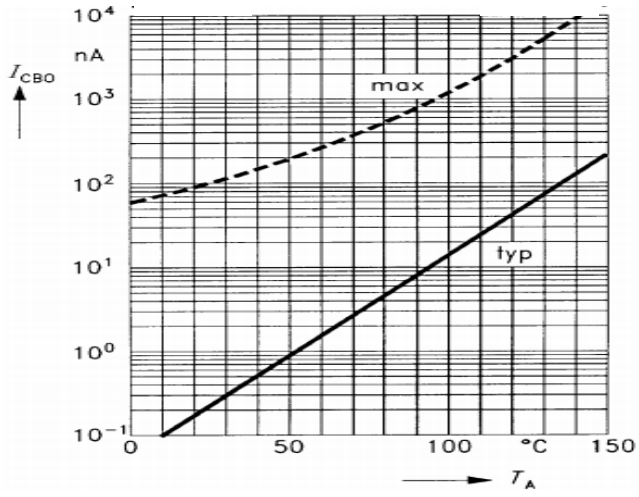
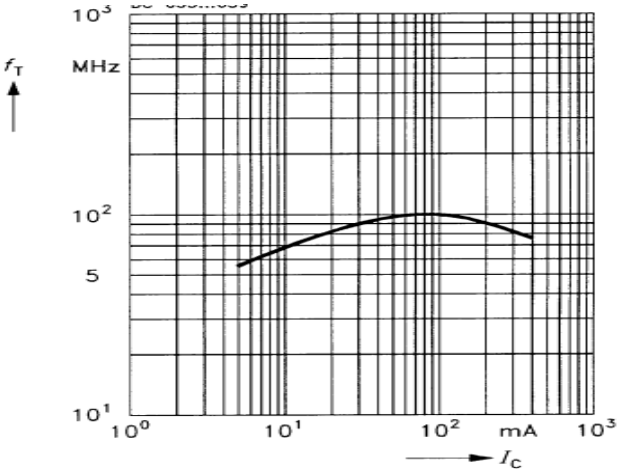


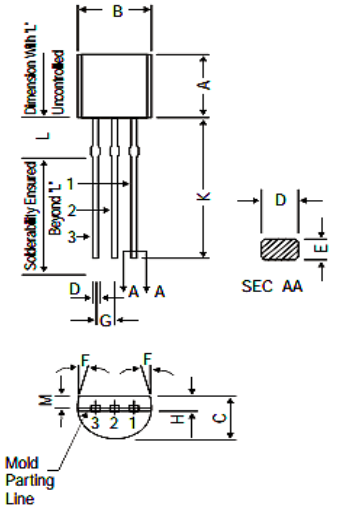
Fig. 6.Transition frequency fT = f (IC) VCE = 10 V, f = 20 MHz



CNL635_40
Rev04 04082023EM

PACKAGE DETAILS

TO-92 Leaded Plastic Package

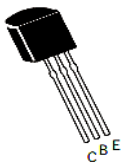


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	
G	1.14	1.40
H	1.20	1.40
K	12.7	
L	1.982	2.082
M	1.03	1.20

All dimensions are in mm

PIN CONFIGURATION

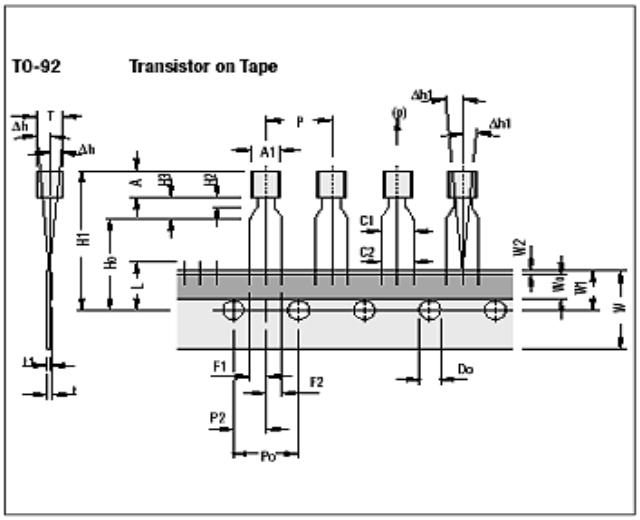
1. Emitter
2. Base
3. Collector

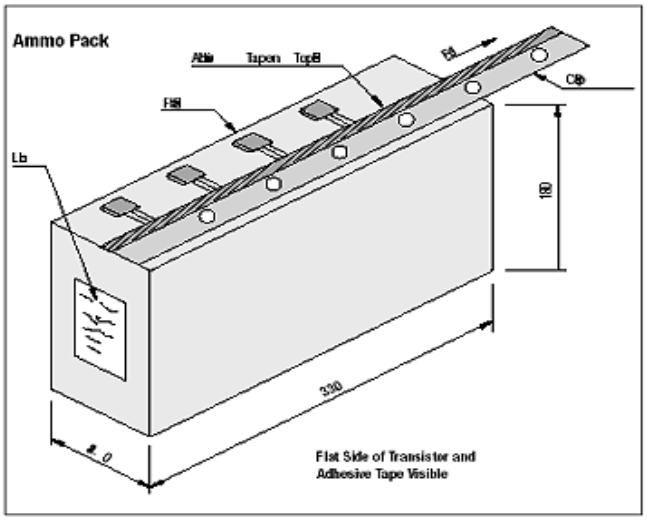


Packaging Information

Package/Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

TO-92 Tape and Ammo Packaging





All Dimensions are in mm

Tape Specifications

		TO-92			
Item description	Symbol	Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[Cr]	P		12.7		±1.0
Feed hole pitch[§1]	Po		12.7		±0.3
Feed hole center to component centre[§2]	P2		6.35		±0.4
Comp. alignment, Side view[§3]	Dh		0	1.0	
Comp. alignment, Front view[§3]	Dh1		0	1.3	
Tape width[Cr]	W		18		±0.5
Hold down tape width[Cr]	Wo		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[Cr]	Do		4		±0.2
Total tape thickness[§4]	t			1.2	
Lead-to-lead distance[Cr]	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelismCr	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 0.6 mm
Cr Critical Dimension.

All Dimensions are in mm

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

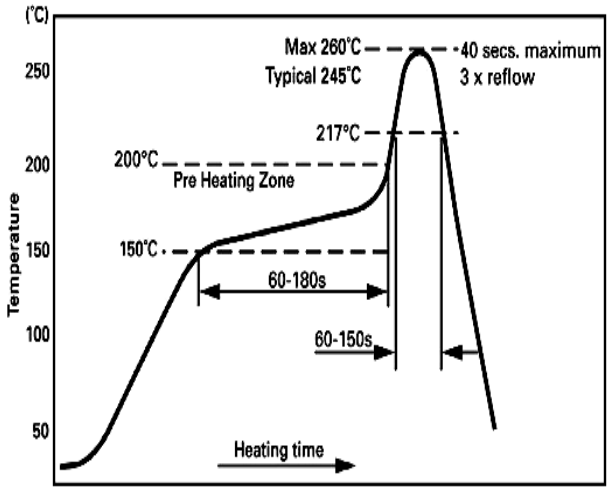
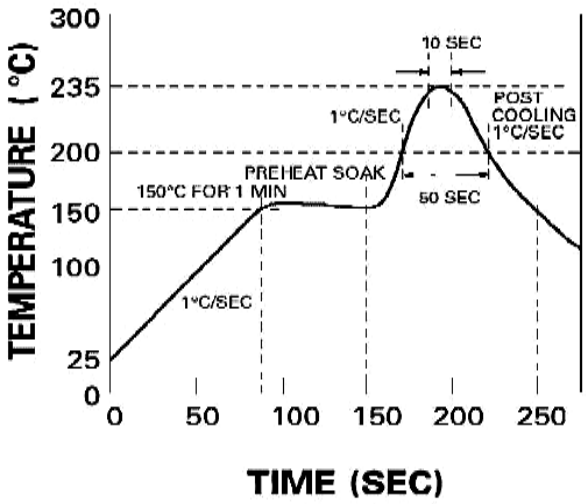


Figure 2

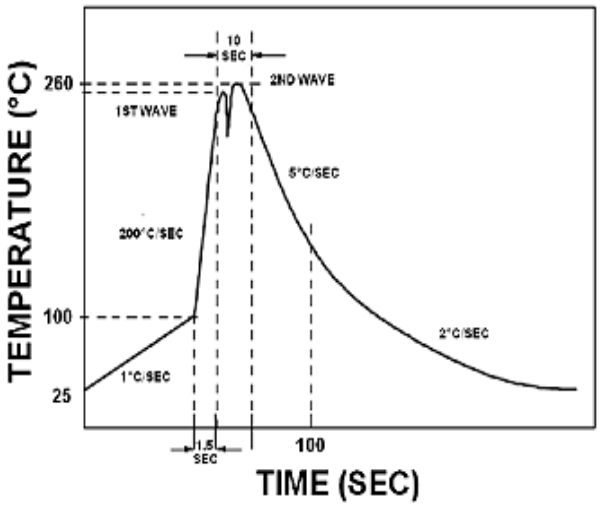


Reflow profiles in tabular form

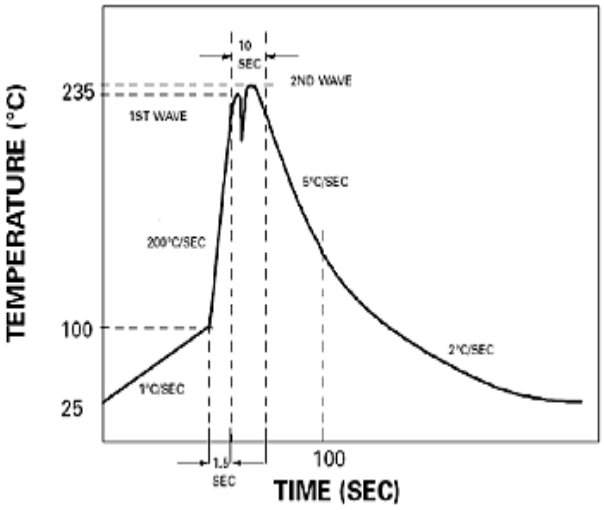
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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