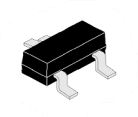
PNP High Voltage Transistor

CMBTA94



SOT-23

SOT-23
Surface Mount
RoHS compliant

FEATURES:

1. High Breakdown Voltage
2. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATIONS:

1. Telephone Switching
2. High Voltage Switch

MAXIMUM RATINGS (Ta=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	400	V
Collector-Emitter Voltage	V_{CEO}	400	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current -Continuous	I_C	200	mA
Collector Current -Pulsed	I_{CM}	300	mA
Collector Power Dissipation	P_C	350	W
Thermal Resistance From Junction To Ambient	$R_{\Theta JA}$	357	°C/W
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55～+150	°C

ELECTRICAL CHARACTERISTICS (Ta=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C=-100μA, I_E=0	400	--	--	V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C=-1mA, I_B=0	400	--	--	V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E=-100μA, I_C=0	5	--	--	V
Collector cut-off current	I_{CBO}	V_{CB}=-400V, I_E=0	--	--	0.1	μA
Collector cut-off current	I_{CEO}	V_{CE}=-400V, I_B=0	--	--	5	μA
Emitter cut-off current	I_{EBO}	V_{EB}=-4V, I_C=0	--	--	0.1	μA
DC current gain	$h_{FE(1)}$	V_{CE}=-10V, I_C=-10mA	80	--	300	--
	$h_{FE(2)}$	V_{CE}=-10V, I_C=-1mA	70	--	--	--
	$h_{FE(3)}$	V_{CE}=-10V, I_C=-100mA	40	--	--	--
	$h_{FE(4)}$	V_{CE}=-10V, I_C=-50mA	40	--	--	--
Collector-emitter saturation voltage	$V_{CE(sat)1}$	I_C=-10mA, I_B=-1mA	--	--	0.2	V
	$V_{CE(sat)2}$	I_C=-50mA, I_B=-5mA	--	--	0.3	V
Base-emitter saturation voltage	$V_{BE(sat)}$	I_C=-10mA, I_B=-1mA	--	--	0.75	V
Transition frequency	f_T	V_{CE}=-20V,I_C=-10mA, f=30MHz	50	--	--	MHz

Note:

1. For PNP device the voltages and current will be negative (-).

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

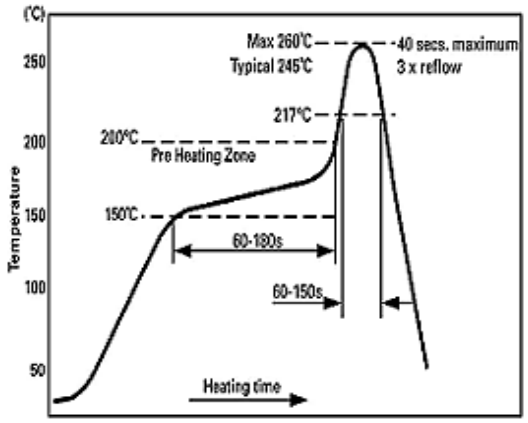
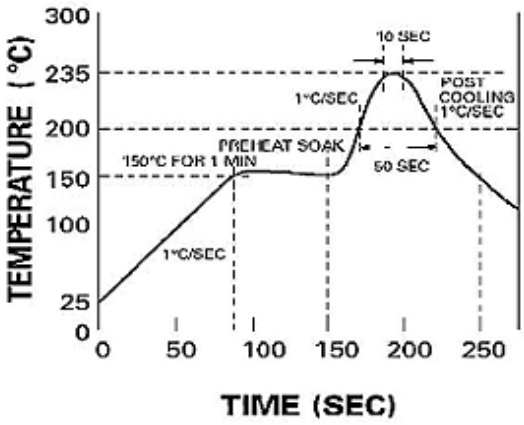


Figure 2

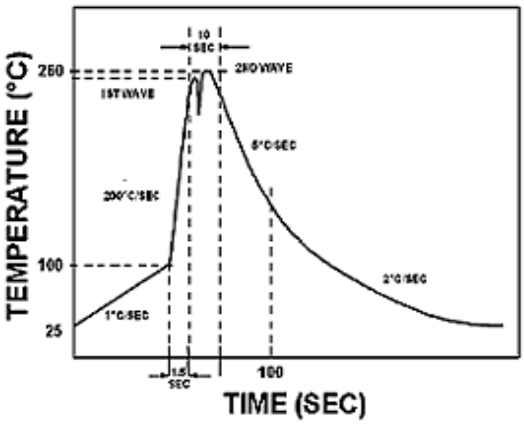


Reflow profiles in tabular form

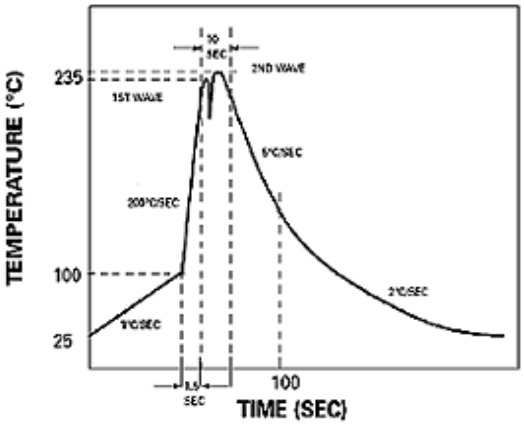
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder.



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

Typical Characteristic curves

Fig 1: Static Characteristic

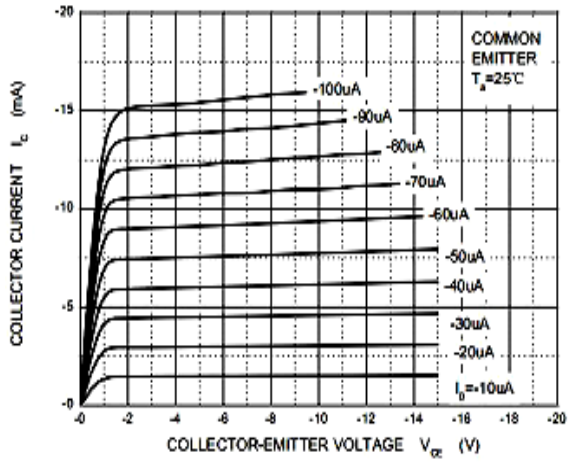


Fig 3: DC Current Gain vs Collector Current

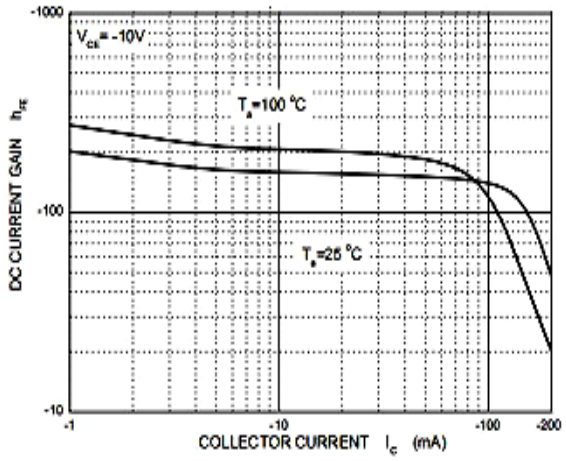


Fig 2: Base-Emitter Saturation Voltage vs Collector Current

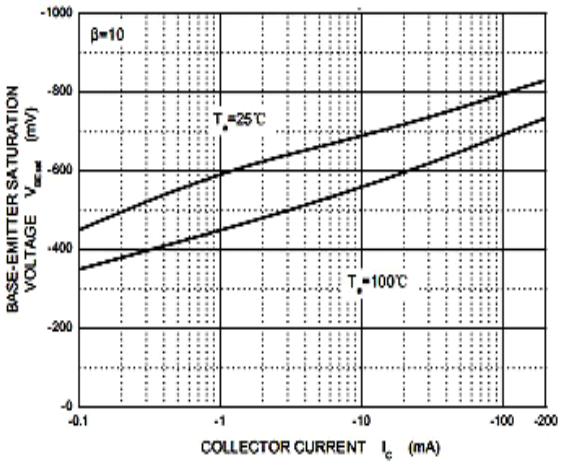
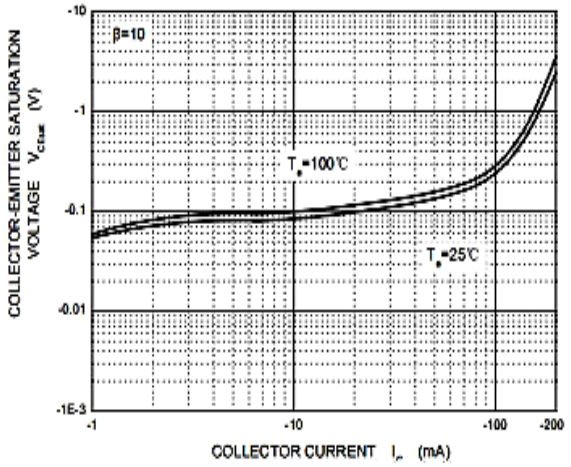


Fig 4: Collector-Emitter Saturation Voltage vs Collector Current



Typical Characteristic curves

Fig 5: Transition Frequency vs Collector Current

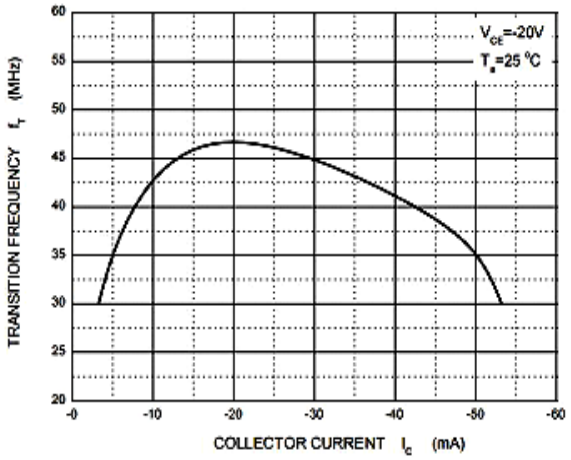


Fig 6: Collector Power Dissipation vs Ambient Temperature

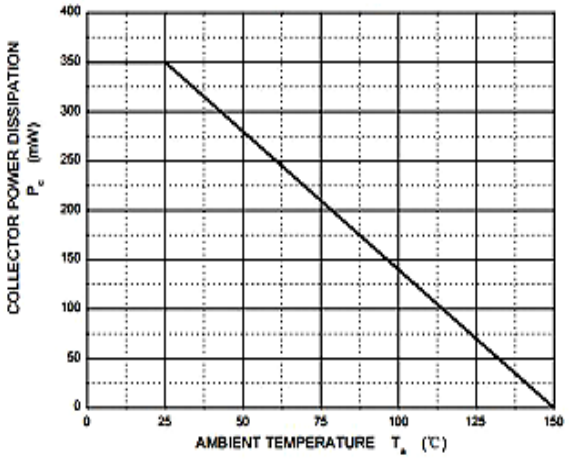
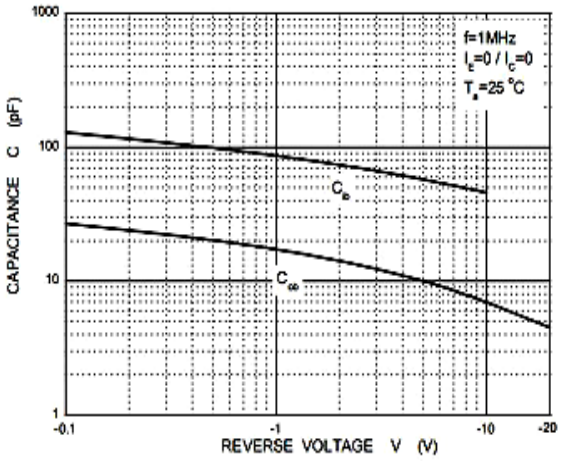
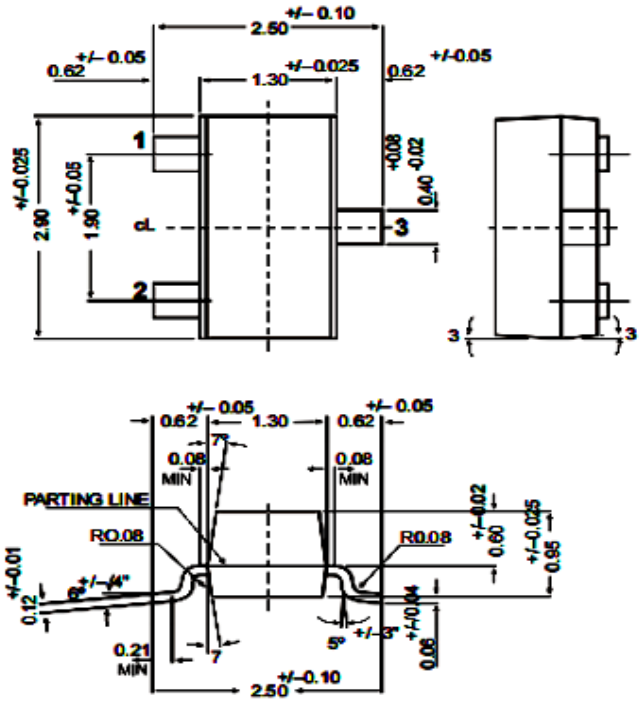


Fig 7: Capacitance vs Reverse Voltage



Package Details

SOT-23 SMD Plastic Package

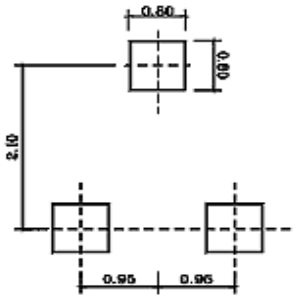


All Dimensions are in mm

Pin Configuration

1. Base
2. Emitter
3. Collector

SOT-23 Suggested Pad Layout



CMBTA94
Rev02_26112022EGL

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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