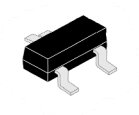
PNP SILICON PLANAR EPITAXIAL TRANSISTORS

CMBT2907
CMBT2907A



SOT-23

SOT-23
Surface Mount
Plastic Package
RoHS compliant

FEATURES:

1. CMBT2907 = 2B
   CMBT2907A = 2F
2. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	SYMBOL	CMBT2907	CMBT2907A	UNIT
Collector–base voltage (open emitter)	V_{CB0}	60	60	V
Collector–emitter voltage (open base)	V_{CE0}	40	60	V
Emitter–base voltage (open collector)	V_{EB0}	5.0		V
Collector current (d.c.)	I_C	600		mA
Power dissipation up to T_{amb} = 25 °C	P_{tot}	250		mW
D.C. current gain (I_C = 500mA; V_{CE} = 10V)	h_{FE}	30	50	
Turn–off switching time (I_{Con} = 150 mA; I_{Bon} = I_{Boff} = 15 mA)	t_{off}	100		ns
Transition frequency at f = 100 MHz (I_C = 50mA; V_{CE} = 20V)	f_T	200		MHz
Storage temperature range	T_{stg}	-55 to +150		°C
Junction temperature	T_j	150		°C

Thermal Resistance

From junction to ambient in free air	$R_{th\ j–a}$	500	K/W

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

Parameter	Symbol	Test Condition	Min	CMBT2907	CMBT2907A	Unit
Collector cut–off current	I_{CB0}	I_E = 0; V_{CB} = 50V	Max	20	10	nA
	I_{CB0}	I_E=0; V_{CB}=50V; T_j = 125°C	Max	20	10	µA
	I_{CEX}	V_{EB}=0,5V; V_{CE}=30V	Max	50		nA
Base current with reverse biased emitter junction	I_{BEX}	V_{EB}=3V; V_{CE}=30V	Max	50		nA
Saturation voltages	V_{CEsat}	I_C=150mA; I_B=15mA	Max	0.4		V
	V_{BEsat}		Max	1.3		V
	V_{CEsat}	I_C=500mA; I_B=50mA	Max	1.6		V
	V_{BEsat}		Max	2.6		V
Collector–base breakdown voltage Open emitter	$V_{(BR)CBO}$	I_C=10µA; I_E=0	Min	60		V
Collector–emitter breakdown voltage Open base	$V_{(BR)CEO}$	I_C=10mA; I_B: 0	Min	40	60	V
Emitter–base breakdown voltage Open collector	$V_{(BR)EBO}$	I_E = 10µA; I_C = 0	Min	5.0		V
D.C. current gain	h_{FE}	I_C = 0,1mA; V_{CE}=10V	Min	35	75	
		I_C = 1mA; V_{CE}=10V	Min	50	100	
		I_C = 10mA; V_{CE}=10V	Min	75	100	
		I_C=150mA; V_{CE}=10V		100 to 300		
		I_C =500mA; V_{CE}=10V	Min	30	50	
Transition frequency at f = 100 MHz Tamb = 25 °C	f_T	I_C= 50mA; V_{CE}=20V	Min	200		MHz
Output capacitance at f =1MHz	C_o	I_E = I_e = 0; V_{CB} = 10V	Max	8.0		pF
Input capacitance at f = 1MHz	C_i	I_C = I_c = 0; V_{EB} = 2V	Max	30		pF

Switching times (between 10% and 90% levels)

Turn–on time when switched to	Delay time	t_d	I_C = 150mA; I_B = 15mA; V_{CC} = 30V	Max	10		ns
	Rise time	t_r		Max	40		ns
	Turn on time(td + tr)	t_{on}		Max	45		ns
Turn–off time when switched from to cut–off with + I_{BM}=15mA	Storage time	t_s	I_C = 150mA; I_B = 15mA; V_{CC} = 6V	Max	80		ns
	Fall time	t_f		Max	30		ns
	Turn–off time (ts + tf)	t_{off}		Max	100		ns

Note:

1. For PNP device voltage and current values will be negative (-).

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

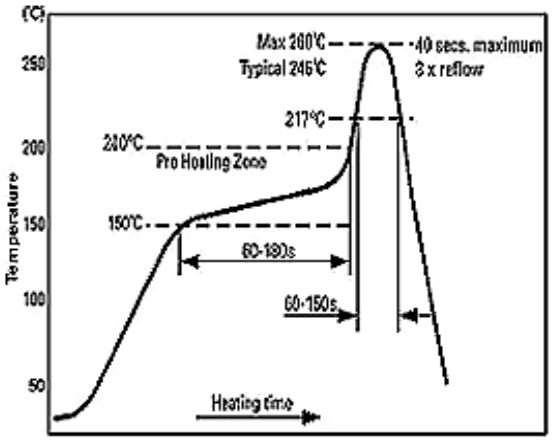
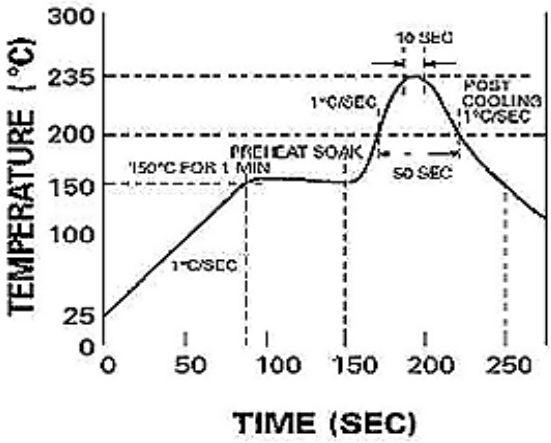


Figure 2

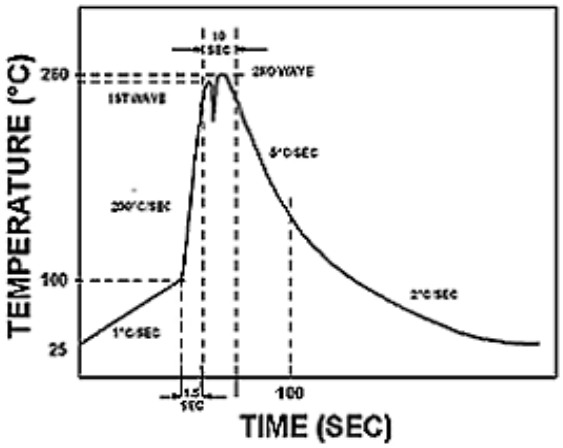


Reflow profiles in tabular form

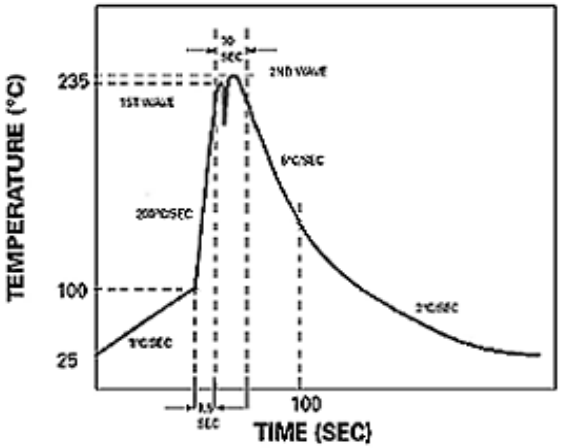
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

Typical Characteristic Curves

Fig 1: Turn-On Time

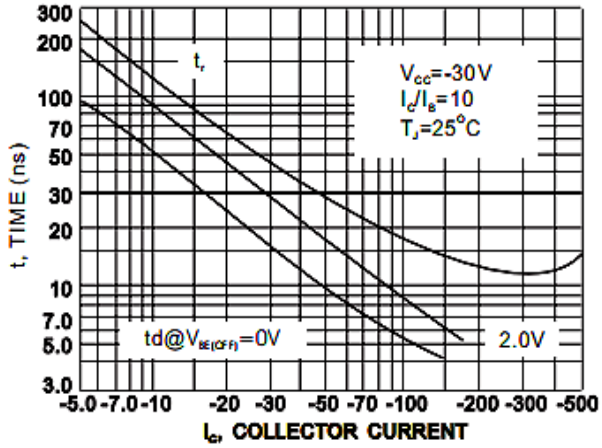


Fig 2: Frequency Effects

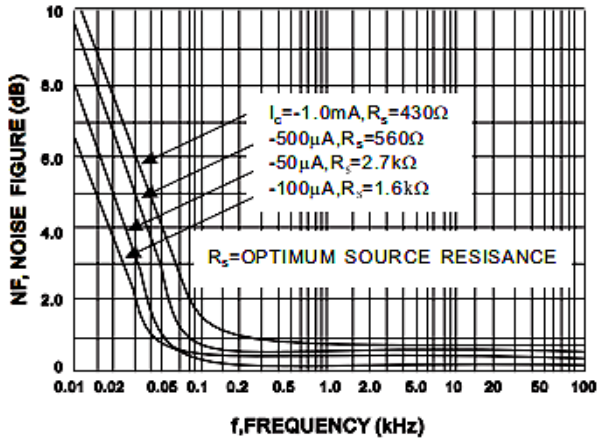


Fig 3: On Voltage

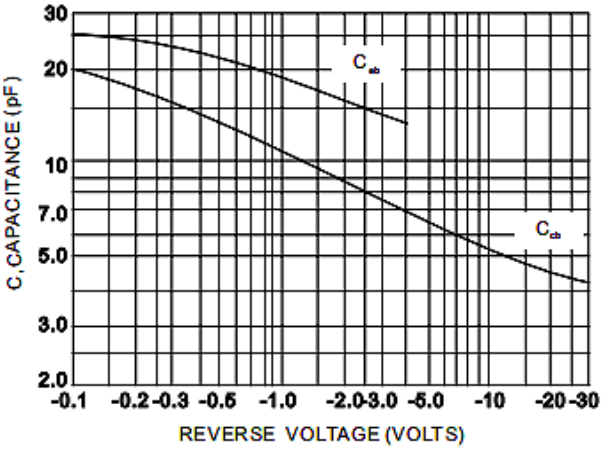


Fig 4: Turn-Off Time

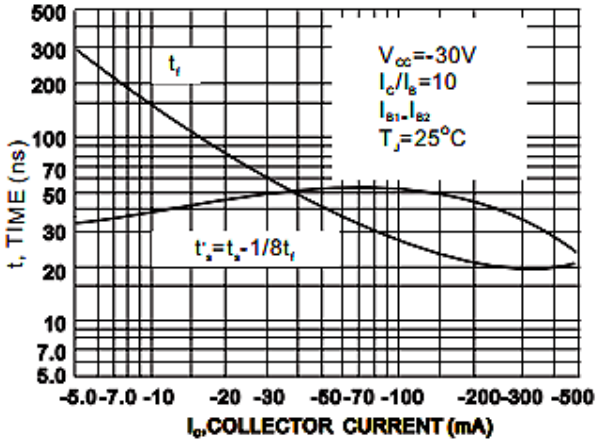


Fig 5: Source Resistance Effects

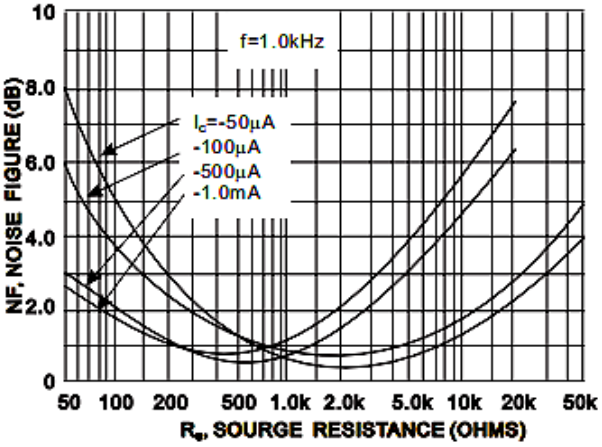
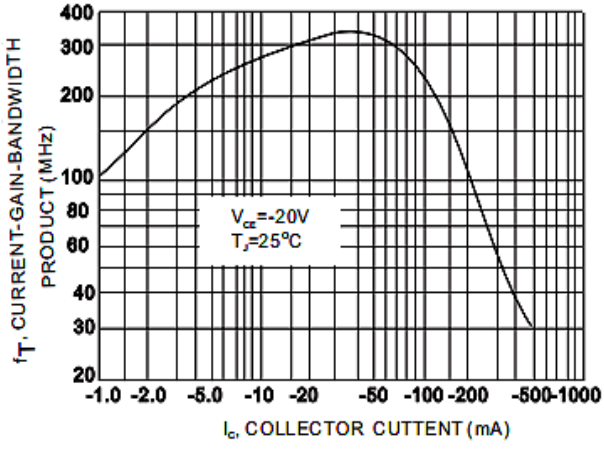


Fig.6: Temperature Coefficients



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Typical Characteristic Curves

Fig 7: On Voltage

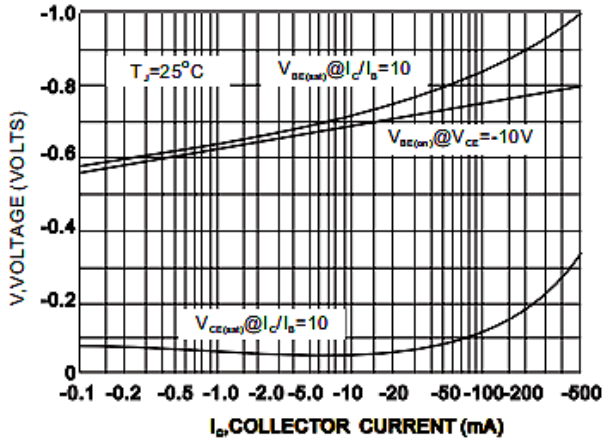


Fig 8: Temperature Coefficients

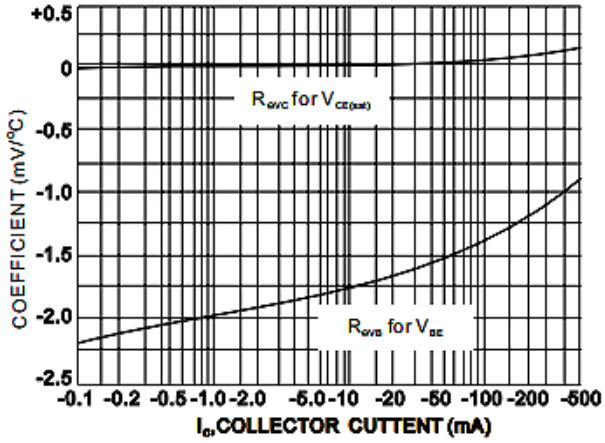


Fig 9: DC Current Gain

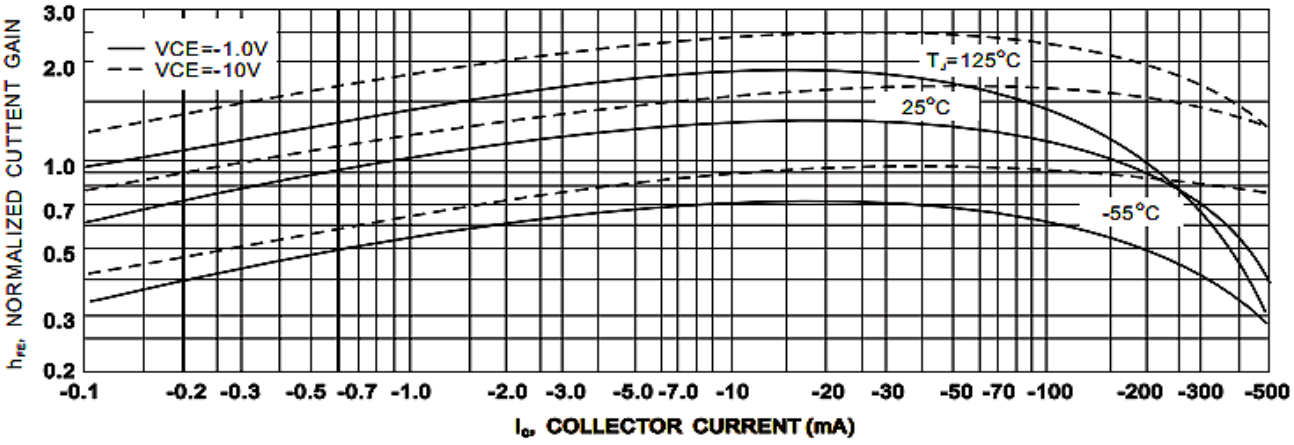
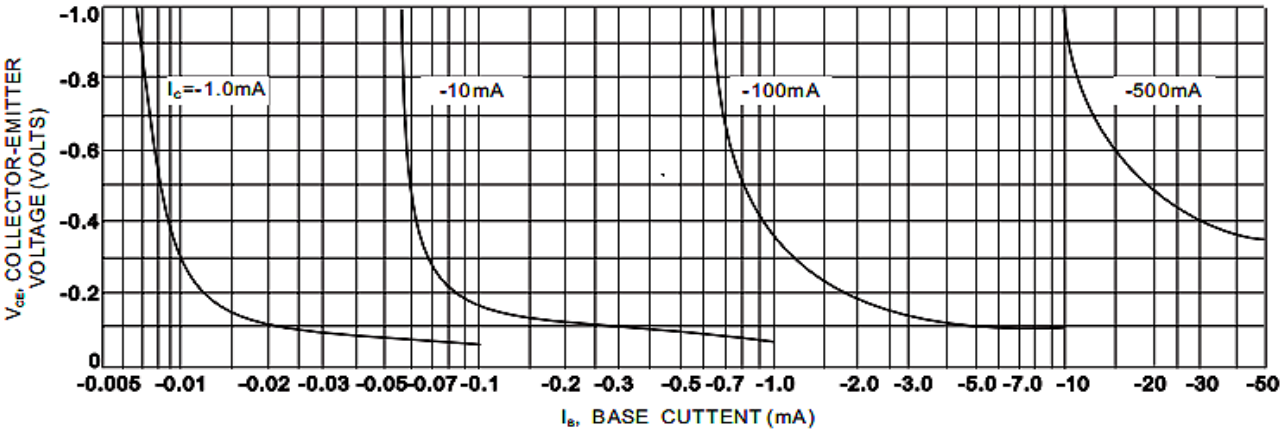
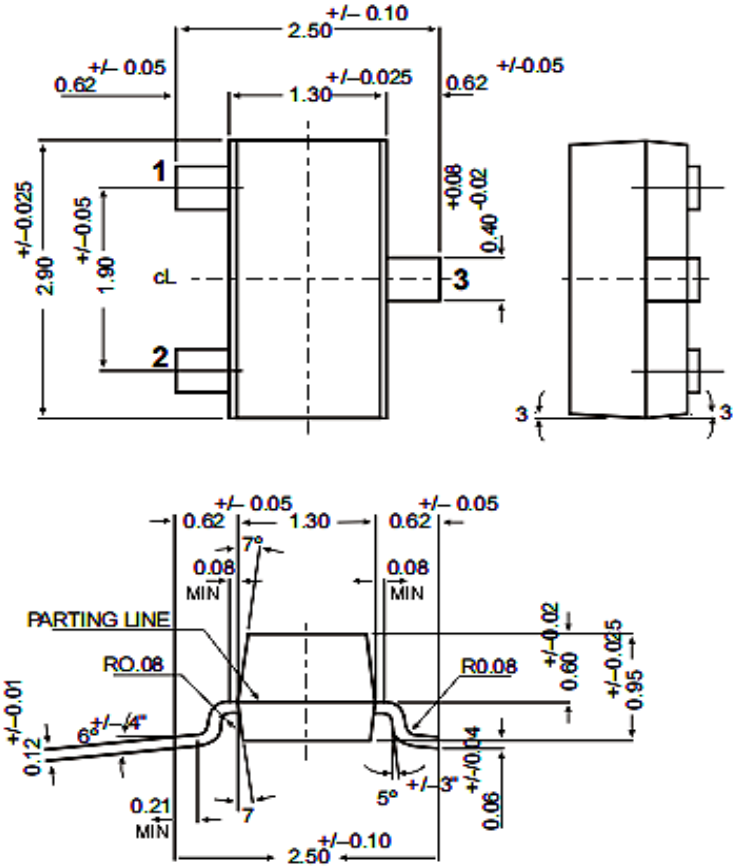


Fig 10: Collector Saturation Region



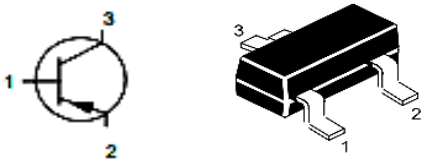
PACKAGE DETAILS

SOT-23 Formed SMD Package



Pin Configuration

1. BASE
2. EMITTER
3. COLLECTOR



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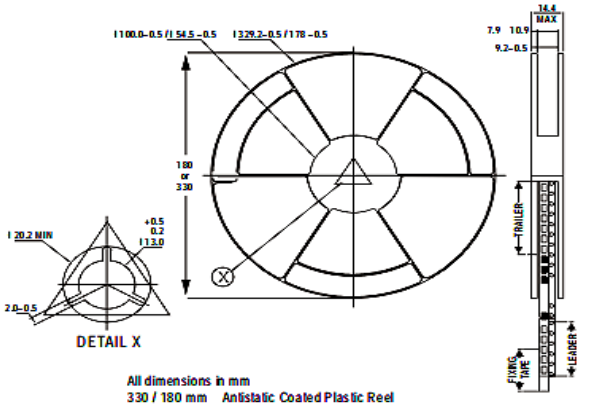
Reel specifications for Packing (13"/7" reels)

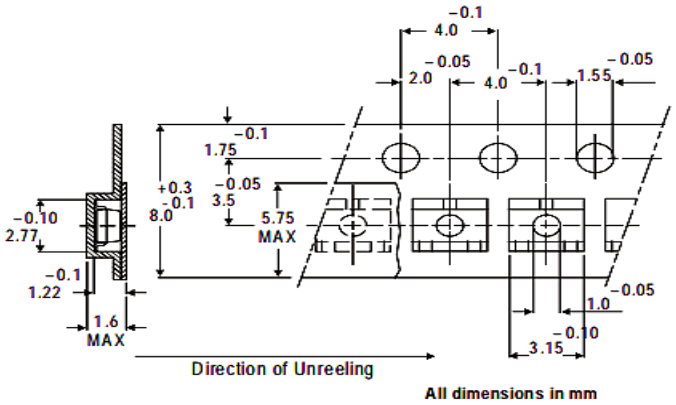


Size of Tape	8mm	8mm
Size of reel	330mm (13")	180mm (7")
No. of Device	10,000 Pcs	3,000 Pcs

NOTES:

1. The bandoier of 330mm reel contains at least 10,000 device.
2. The bandoier of 180mm reel contains at least 3,000 device.
3. No more than 0.5% missing device/reel 50 empty compartments for 330mm reel. 15 empty compartments for 180mm reel.
4. Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.
5. The carrier tape (leader) starts with at least 75 empty positions (equivalent to 330 mm). In order to fix the carrier tape a self adhesive tape of 20 to 50 mm is applied. At the end of the bandolier at least 40 empty positions (equivalent to 160 mm) are there.

Tape Specification for SOT-23 Surface Mount Device



Packing Detail

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
SOT-23 T&R	3K/reel	136 gm/3K pcs	3" x 7.5" x 7.5"	12.0K	17" x 15" x 13.5"	192.0K	12 kgs
			9" x 9" x 9"	51.0K	19" x 19" x 19"	408.0K	28 kgs
	10K/reel	415 gm/10K pcs	13" x 13" x 0.5"	10.0K	17" x 15" x 13.5"	300.0K	16 kgs

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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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