

## NPN/PNP SILICON PLANAR EPITAXIAL TRANSISTORS

NPN CIL187  
PNP CIL188



TO-92

TO-92  
Plastic Package  
RoHS compliant

### FEATURE:

1. Complementary CIL 188
2. This product is available in AEC-Q101 Compliant and PPAP Capable also.

**Note:** For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

**APPLICATIONS:** Intended For Low Voltage , High Current Output Pair Application

### ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Collector Emitter Voltage ( $V_{BE}=0$ )	$V_{CES}$	25	V
Collector Emitter Voltage ( Open Base)	$V_{CEO}$	15	V
Emitter Base Voltage ( Open Collector)	$V_{EBO}$	5	V
Collector Current	$I_C$	700	mA
Collector Current ( Peak Value )	$I_{CM}$	1	A
Base Current	$I_B$	100	mA
Base Current (Peak Value)	$I_{BM}$	200	mA
Total Power Dissipation @ Ta=25°C	$P_{TA}$	625	mW
Operating And Storage Junction Temperature Range	$T_j, T_{stg}$	-55 to +150	°C

### ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector Cut off Current	$I_{CBO}$	$V_{CB}=25V, I_E = 0$	--	--	10	$\mu A$
		$V_{CB}=25V, I_E = 0, I_C = 1mA, T_j = 150^\circ C$	--	--	1	mA
Emitter Cut off Current	$I_{EBO}$	$V_{EB}=5V, I_C = 0$	--	--	10	$\mu A$
Base Cut on Voltage	$V_{BE(on)}$	$I_C = 1A, V_{CE} = 1V$	--	--	1	V
Collector Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 1A, I_B = 100mA$	--	--	0.5	V
DC Current Gain	$h_{FE}$	$V_{CE}=10V, I_C=5mA$	50	--	--	
		$V_{CE}=1V, I_C=300mA$	100	--	300	
		$V_{CE}=1V, I_C=1A$	40	--	--	

### DYNAMIC CHARACTERISTICS

Transition Frequency	$f_T$	$I_C=10mA, V_{CE}=2V$	--	270	--	MHz	
Collector Capacitance	$C_c$	$I_E=0, V_{CB}=5V, f=1MHz$	CIL187	--	10	--	pF
			CIL188	--	30	--	pF

Note: For PNP device voltage and current values will be negative (-)

CIL187\_188

Rev02 19072022E

### Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

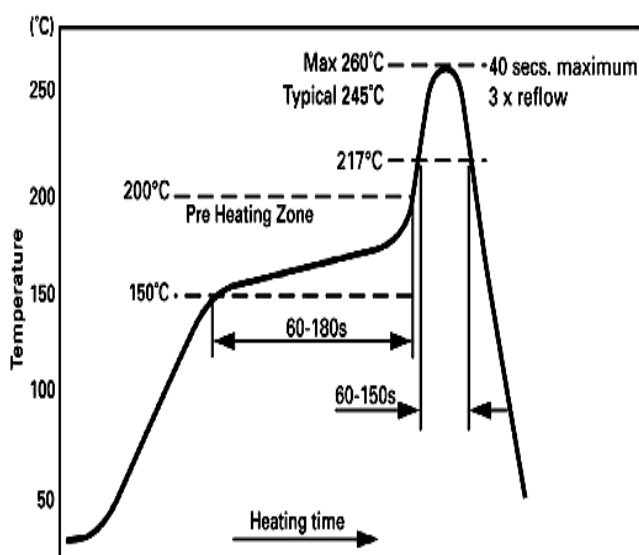
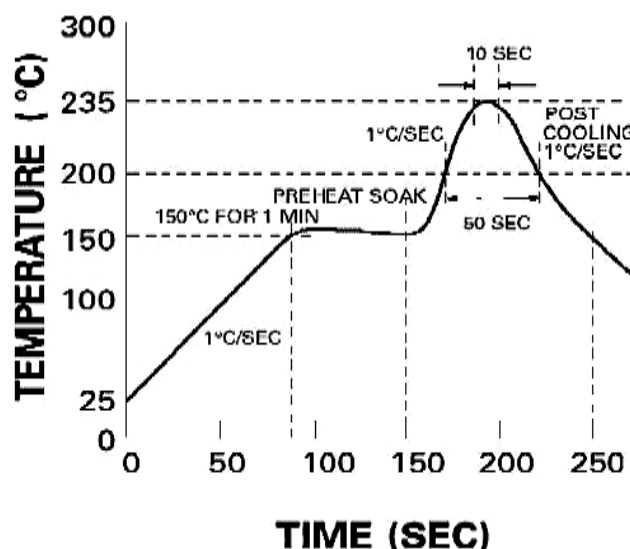


Figure 2



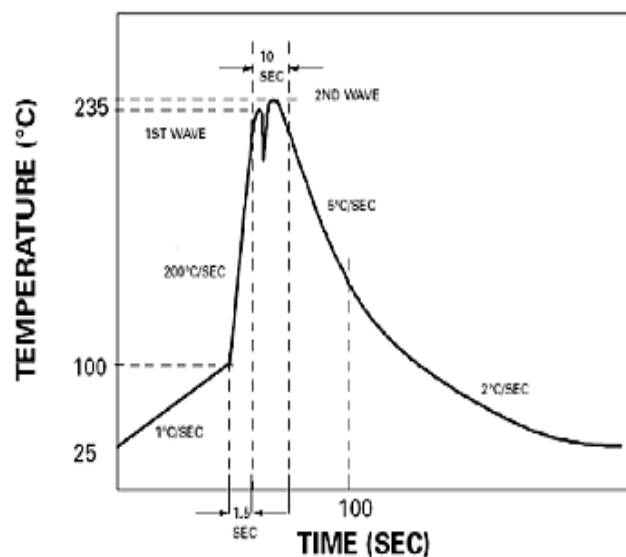
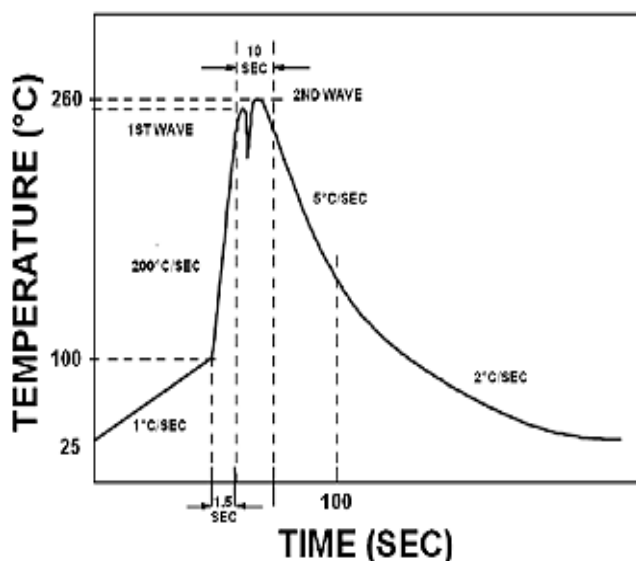
Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
<b>Preheat</b>		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Time	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

### Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used

The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



### Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

## TYPICAL CHARACTERISTIC CURVES

Figure 1. DC Current Gain

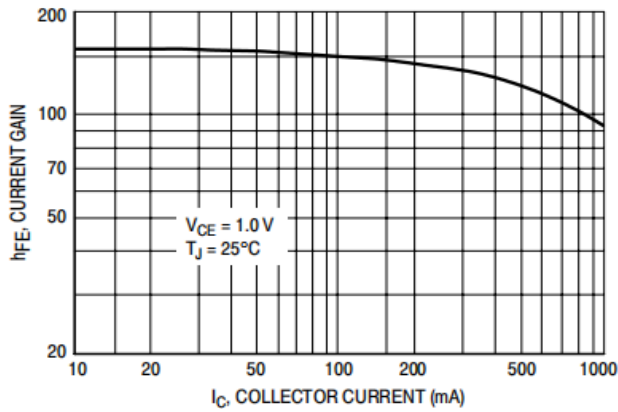


Figure 4. Temperature Coefficient

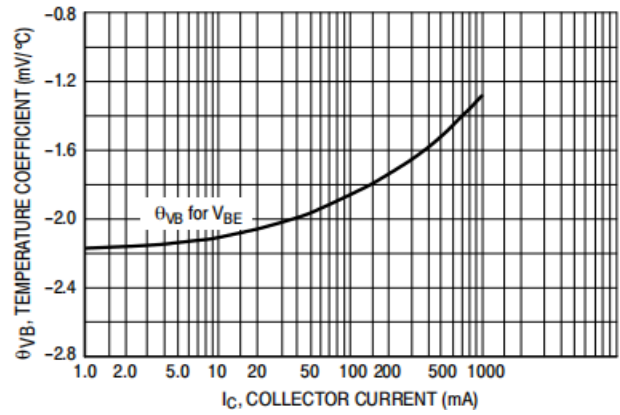


Figure 2. Collector Saturation Region

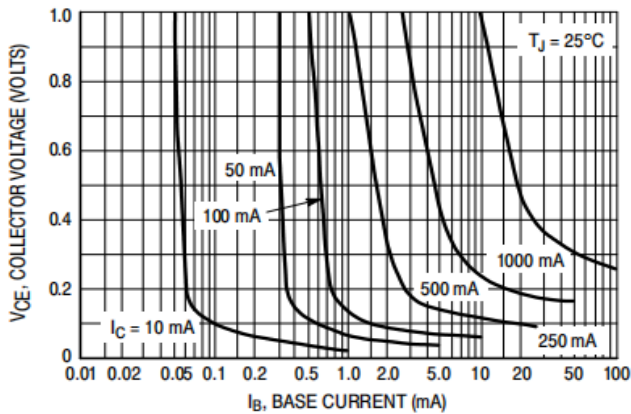


Figure 5. Current-Gain — Bandwidth Product

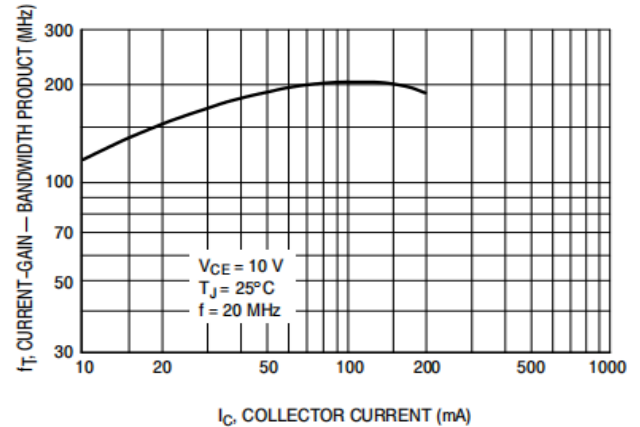


Figure 3. "On" Voltages

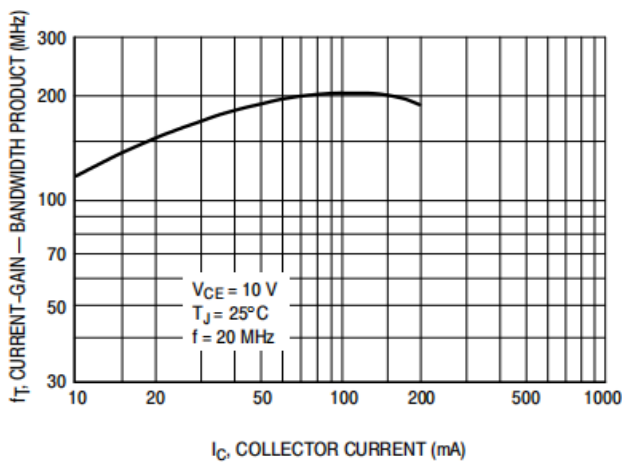
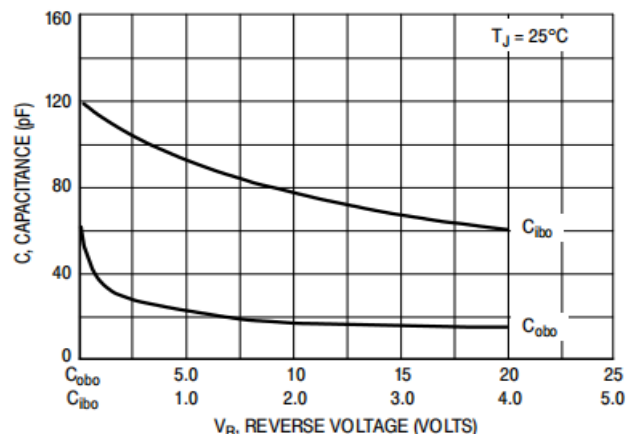
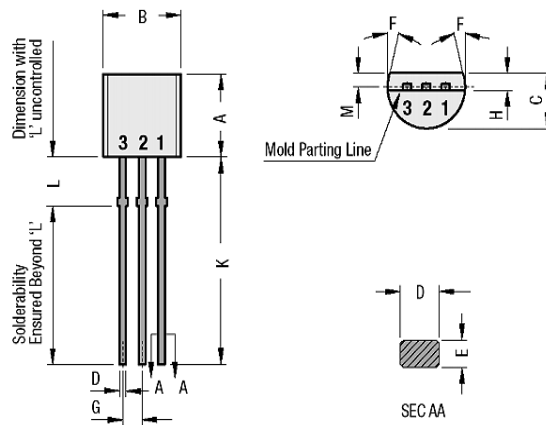


Figure 6. Capacitance



## PACKAGE DETAILS

### TO-92 Leaded Plastic Package

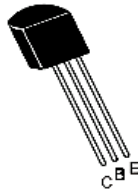


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	
G	1.14	1.40
H	1.20	1.40
K	12.7	
L	1.982	2.082
M	1.03	1.20

All dimensions are in mm

### PIN CONFIGURATION

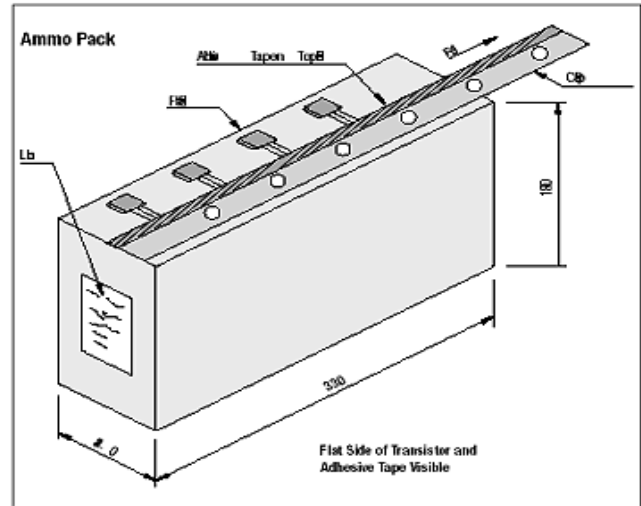
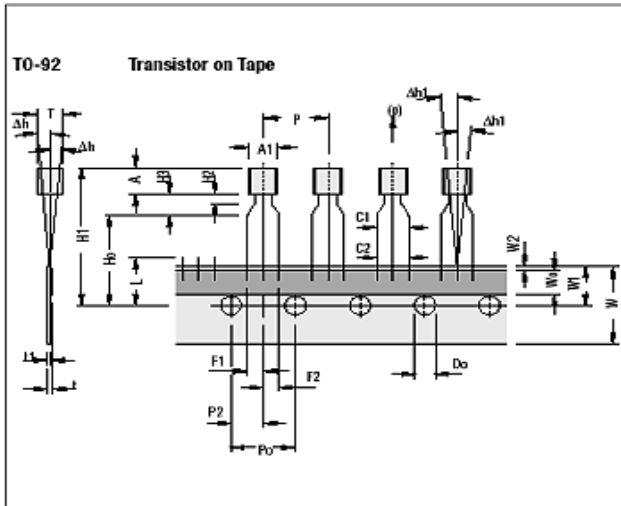
1. Emitter
2. Base
3. Collector



### Packaging Information

Package/Case Type	Packaging Type	Std. Packing		Inner Carton		Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

TO-92 Tape and Ammo Packaging



All Dimensions are in mm

Tape Specifications

Item description	Symbol
Body width	A1
Body height	A
Body thickness	T
Pitch of component <sup>Cr</sup>	P
Feed hole pitch <sup>§1</sup>	Po
Feed hole center to component centre <sup>§2</sup>	P2
Comp. alignment, Side view <sup>§3</sup>	Dh
Comp. alignment, Front view <sup>§3</sup>	Dh1
Tape width <sup>Cr</sup>	W
Hold down tape width <sup>Cr</sup>	W0
Hole position	W1
Hold-down tape position	W2
Lead wire clinch height	Ho
Component height	H1
Length of snipped leads	L
Feed hole diameter <sup>Cr</sup>	Do
Total tape thickness <sup>§4</sup>	t
Lead-to-lead distance <sup>Cr</sup>	F1, F2
Stand off	H2
Clinch height	H3
Lead parallelism <sup>Cr</sup>	C1-C2
Pull-out force	(p)

TO-92			
Min	Nom	Max	Tol
4.45		5.20	
4.32		5.33	
3.18		4.19	
	12.7		±1.0
	12.7		±0.3
	6.35		±0.4
	0	1.0	
	0	1.3	
	18		±0.5
	6		±0.2
	9		+0.7 -0.5
0.0		0.7	
	16		±0.5
		24.0	
		11.0	
	4		±0.2
		1.2	
	2.4	2.7	
	0.45	1.45	
		3.0	
		0.22	
6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.

§2 To be measured at bottom of clinch.

§3 At top of body.

§4 t1 = 0.3 – 0.6 mm

Cr Critical Dimension.

All Dimensions are in mm



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An IATF 16949, ISO9001 and ISO 14001 Certified Company



### Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

#### Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

#### Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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## Customer Notes

### Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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