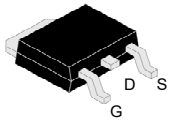
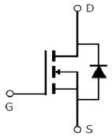
60V N-Channel MOSFET

CDD58N06



TO-252 (DPAK)



TO-252 (DPAK)
Surface Mount
Plastic Package
RoHS compliant

General Description

These N-Channel enhancement mode power field effect transistors are produced using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance and gate charge, provide superior switching performance and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for UPS, power switching and a wide variety of other applications.

FEATURES:

1. Low on-state resistance
2. Fast switching
3. High Power and current ωhanding capability
4. Lead free product

$I_{D(max)}$=58A,
$BV_{DS}S$=60V,
$R_{DS(on)}$ = 11mΩ @V_{GS} = 10V

APPLICATION:

1. High Current, High Speed
2. Motor Control, Audio Amplifiers
3. DC-DC & DC-AC Converters

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ℃)

Parameters	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current ,V_{GS} @ 10V (Tc =25°C) [1]	I_D	58	A
Continuous Drain Current ,V_{GS} @ 10V (Tc =100°C) [1]		48	
Pulsed Drain Current [2]	I_{DM}	240	A
Power Dissipation (25℃)	P_D	85	W
Power Dissipation (25℃) Derating Factor		0.57	W/ºC
Single pulse avalanche energy [4]	E_{AS}	300	mJ
Thermal Resistance, Junction to Case [3]	$R_{\theta JC}$	2	ºC/W
Thermal Resistance, Junction to Ambient [5, 6]	$R_{\theta JA}$	62	ºC/W
Operating and Storage Temperature Range	T_j,T_{STG}	-55 to +175	ºC

ELECTRICAL CHARACTERISTICS at T_a = 25 ℃(Unless otherwise specified)

Parameter	Symbol	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	V_{DS} =0V, V_{GS}=± 20V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}= V_{GS}, I_D= 250μA	1	-	2.5	V
Static Drain-Source on-Resistance	$R_{DS(on)}$**	V_{GS} =10V, I_D=30 A	-	11	15	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=30A	20	-	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} =50V, V_{GS} = 0V, f = 1.0MHz	-	2740	-	pF
Output Capacitance	C_{oss}		-	185	-	pF
Reverse Transfer Capacitance	C_{rss}		-	90	-	pF
Total Gate Charge	Q_g	V_{DS} =30V, I_D =30A, V_{GS} =10V	-	46	-	nC
Gate-Source Charge	Q_{gs}		-	9	-	nC
Gate-Drain(“Miller”) Charge	Q_{gd}		-	16	-	nC
Switching Characteristics						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}= 30V, I_D =30A, R_G=2.5Ω, V_{GS}=10 V	-	15	-	ns
Turn-on Rise Time	t_r		-	38	-	ns
Turn-off Delay Time	$t_{d(off)}$		-	51	-	ns
Turn-off Fall Time	t_f		-	23	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain to			-	-	58	A
Maximum Pulsed Drain to Source			-	-	232	A
Drain to Source Diode Forward	V_{SD}	V_{GS}=0V, I_S=30A	-	0.9	1.3	V
Reverse Recovery Time	t_{rr}	I_F=30A, dI/dt=100A/μs, T_J =25°C	-	55	-	ns
Reverse Recovery Charge	Q_{rr}		-	63	-	nC

Notes:

1. Based on $T_{J(MAX)}$=175°C in a TO252 package, using junction-to-case thermal resistance
2. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.
3. Surface Mounted on FR4 Board, t ≤ 10 sec.
4. EAS condition : T_j=25℃,V_{DD}=20V,V_G=10V,L=0.5mH,R_g=25Ω，I_{AS}=35A
5. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
6. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

Typical electrical and thermal characteristics：

Figure 1: Typical Output Characteristics

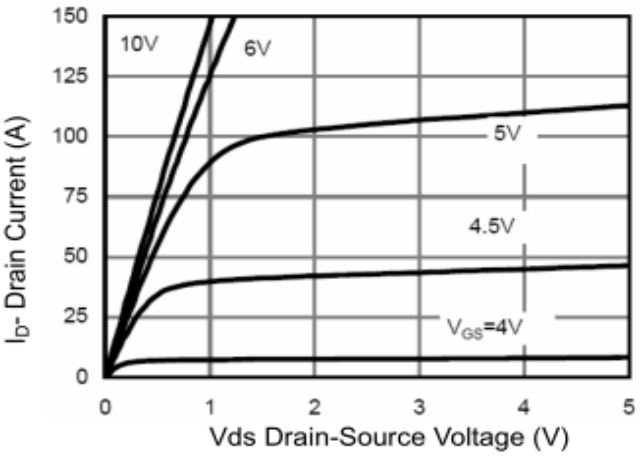


Figure 2: Typical Transfer Characteristics

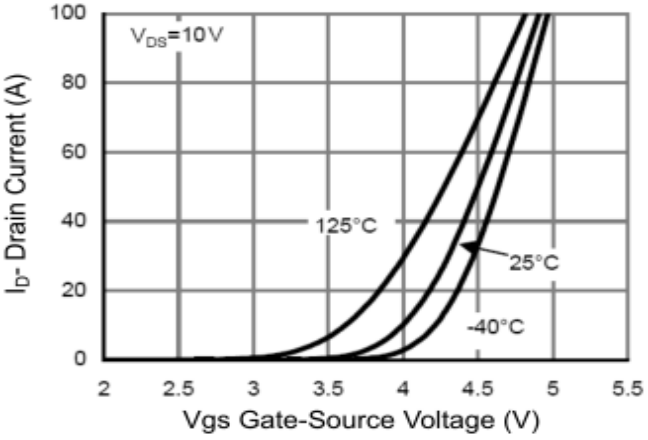


Figure 3: Body-Diode Characteristics

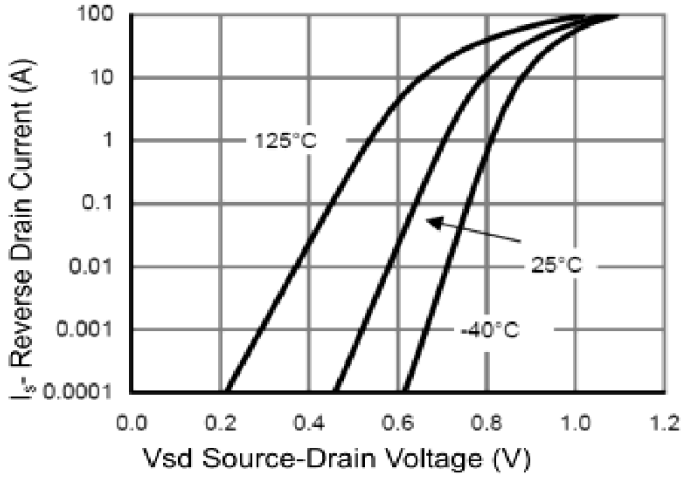


Figure 4: On-Resistance vs. Junction Temperature

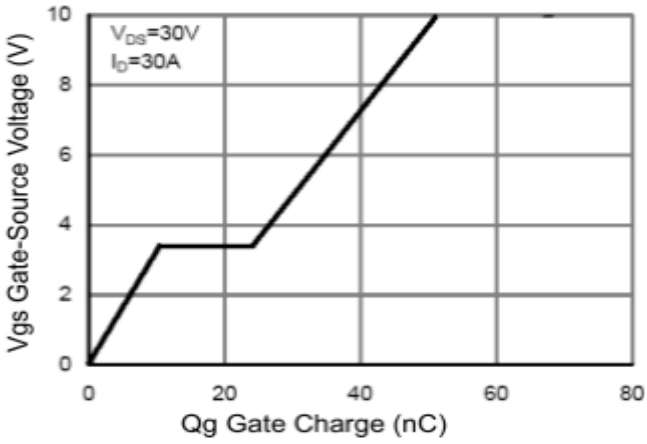


Figure 5: Capacitance Characteristics

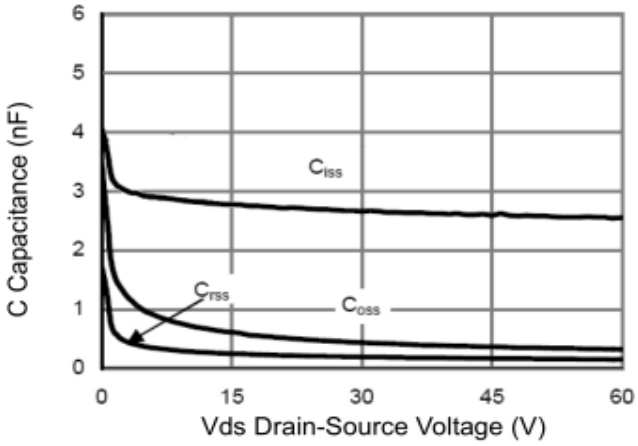
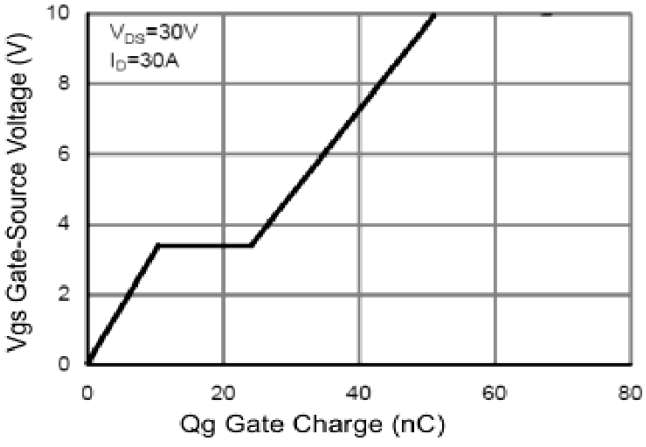


Figure 6: Gate-Charge Characteristics



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Typical electrical and thermal characteristics：

Figure 7: Maximum Forward Biased Safe Operating Area

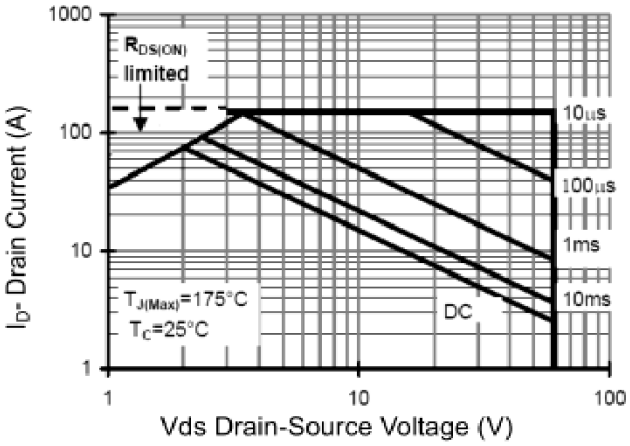


Figure 8: Current De-rating

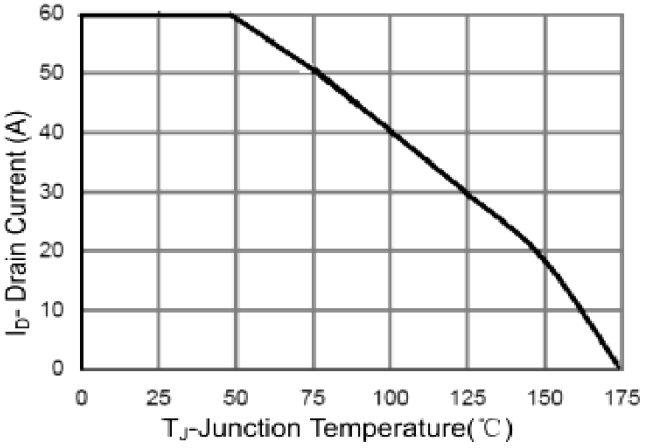
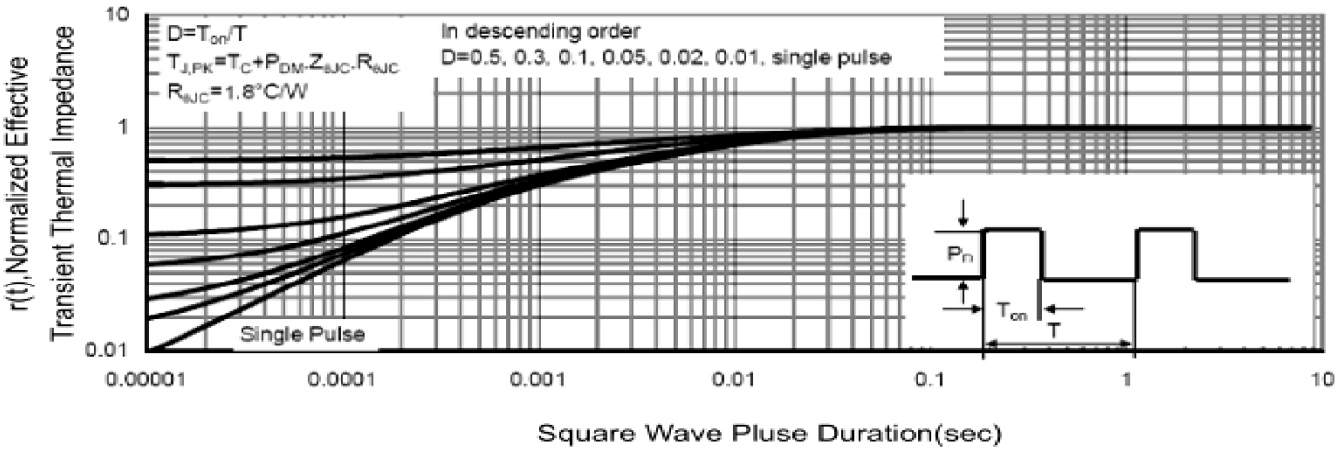


Figure 9: Normalized Maximum Transient Thermal Impedance



Test circuits and Waveforms:

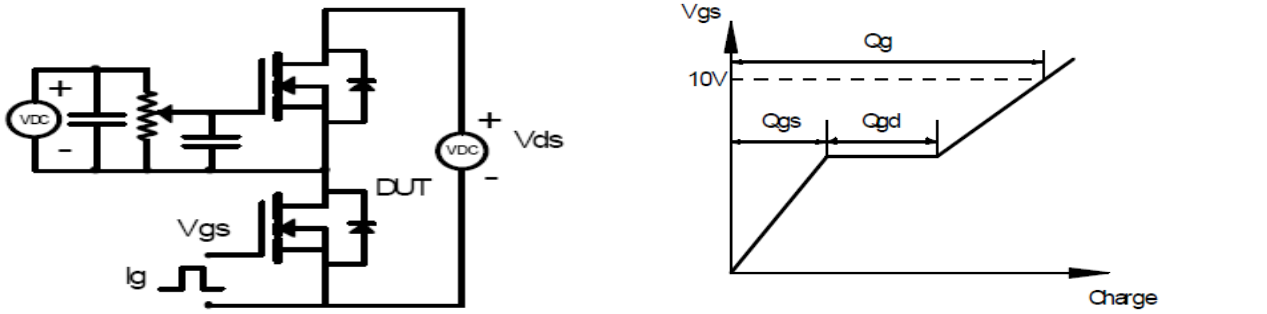


Fig 1: Gate Charge Test Circuit & Waveform

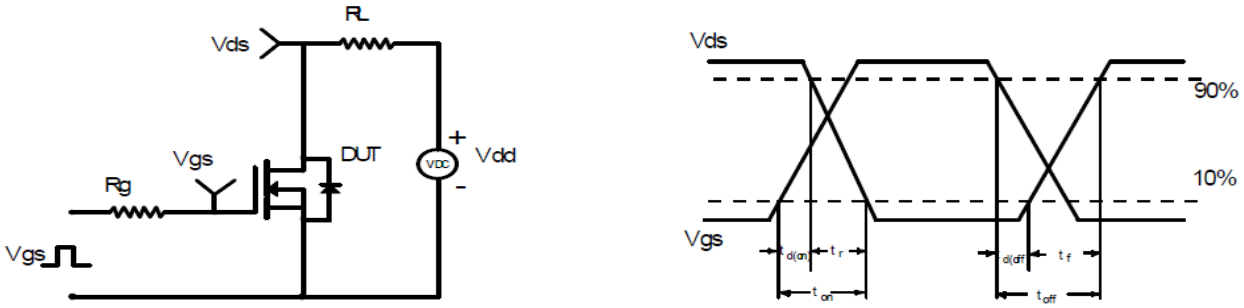


Fig 2: Resistive Switching Test Circuit & Waveforms

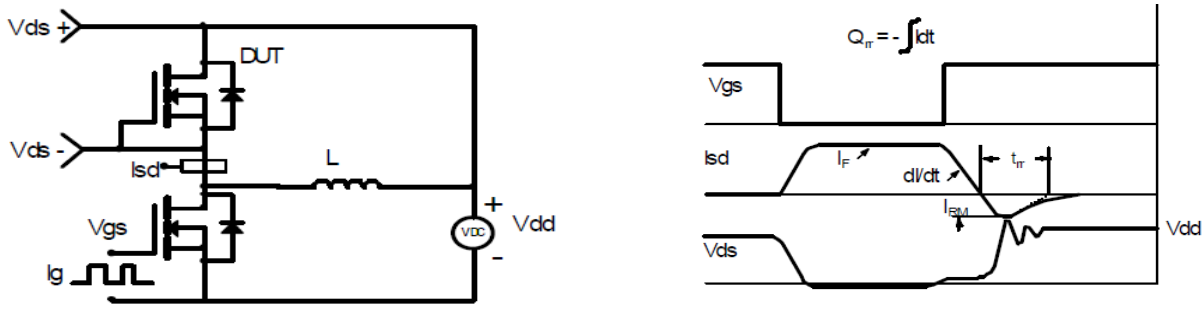


Figure 3. Reverse recovery test circuit and waveform

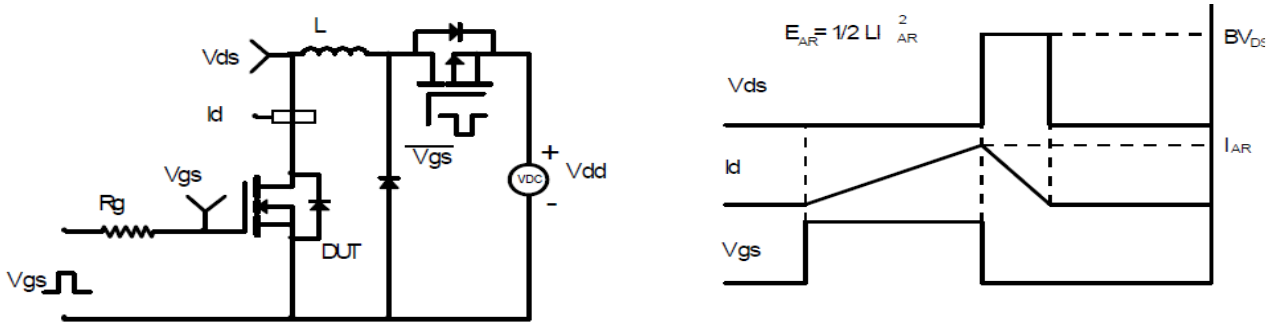


Figure 4. EAS test circuit and waveform

Typical Performance Characteristics

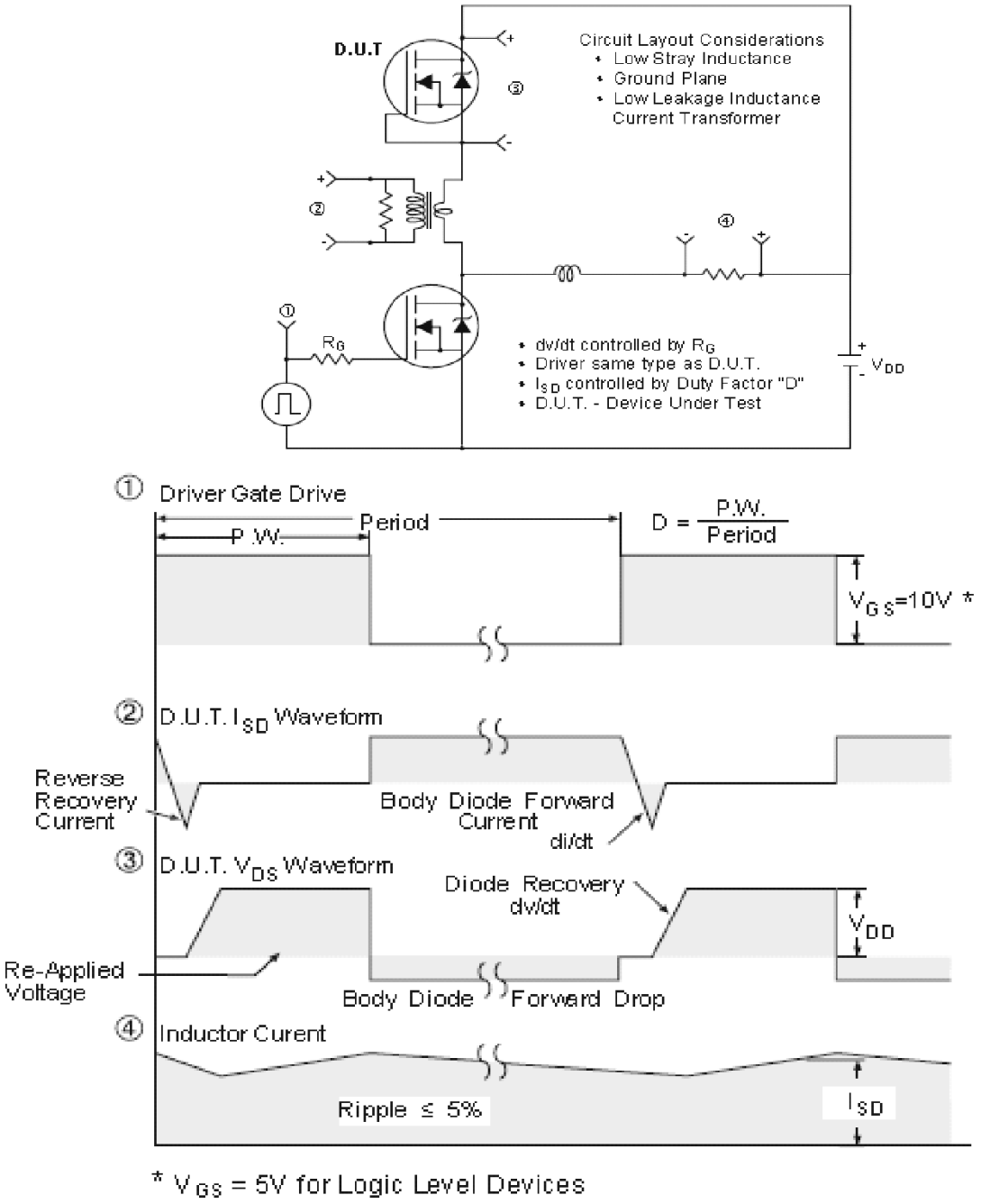
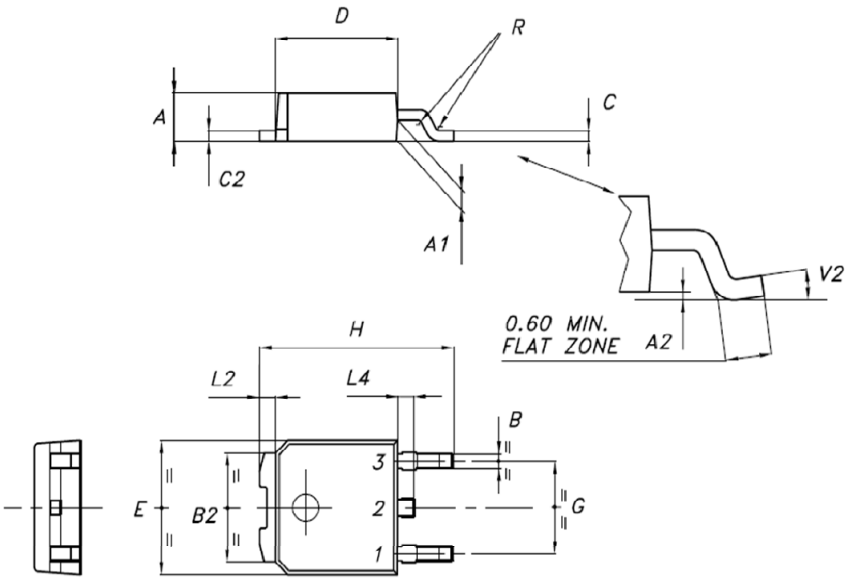


Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

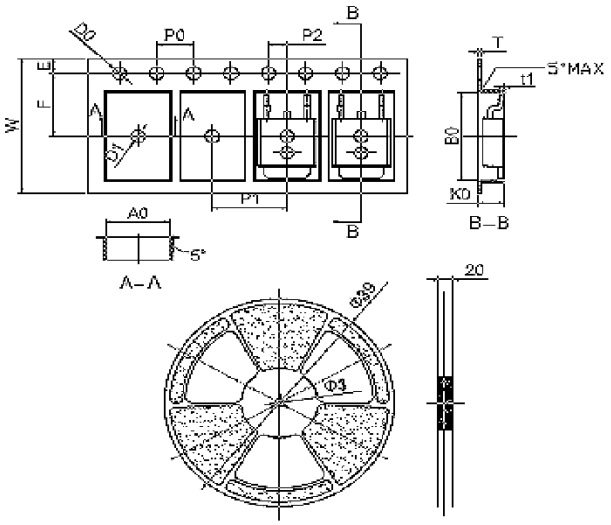
Package Details:

TO-252 (D-PAK)



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

Reel Specification-TO-252 (D-PAK)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

Packing	Reels (Pcs)	Per Carton (Pcs)	Tape& Reel
Taping	2,500	25,000	13 inch

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

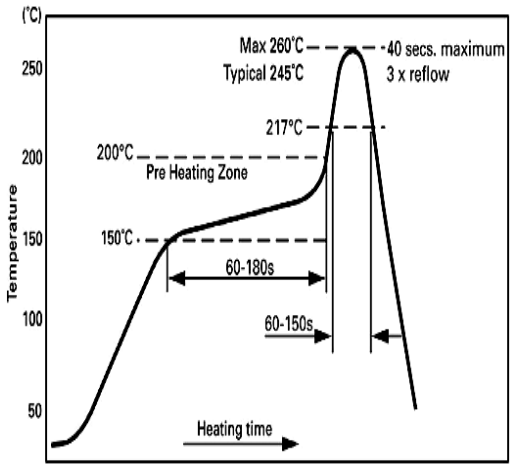
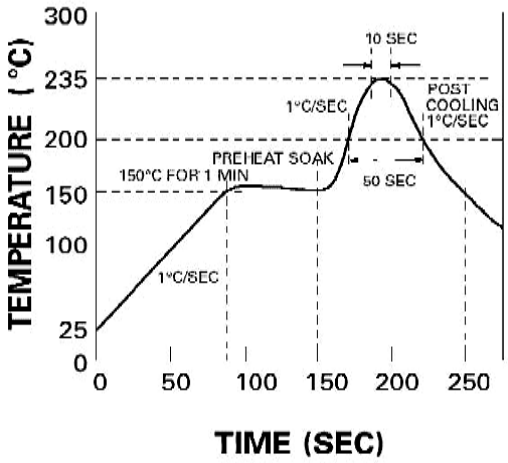


Figure 2

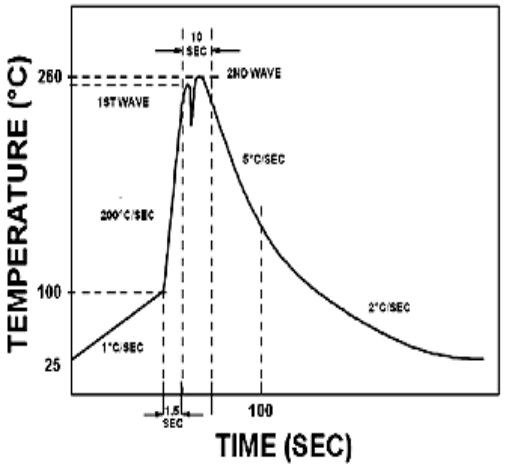


Reflow profiles in tabular form

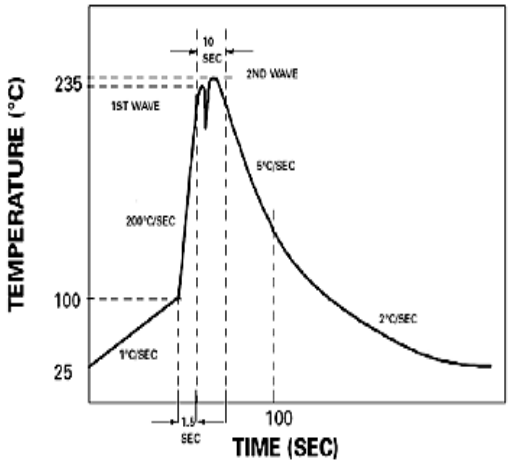
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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