



8A TRIACs BTB08



TO-220 Leaded Plastic Package RoHS compliant

TO-220

## **GENERAL DISCRIPTION:**

With high ability to withstand the shock loading of large current, BTB08 series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load. From all three terminals to external heatsink, BTB08 provides a rated insulation voltage of 2500  $V_{RMS}$ , and BTB08 provides a rated insulation voltage of 2000  $V_{RMS}$ , complying with UL standards (File ref: E252906). All the packages above are RoHS compliant.(2011/65/EU)

## **MAIN FEATURES**

SYMBOL	VALUE	UNIT
I <sub>T(RMS)</sub>	8	Α
$V_{DRM}/V_{RRM}$	600/800/1200	V

## **ABSOLUTE MAXIMUM RATINGS** (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Storage junction temperature range	$T_{stg}$	-40 to +150	°C
Operating junction temperature range	$T_j$	-40 to +125	°C
Repetitive peak off-state voltage (T <sub>j</sub> =25°C)	$V_{DRM}$	600/800/1200	V
Repetitive peak reverse voltage (T <sub>j</sub> =25°C)	$V_{RRM}$	600/800/1200	V
Non repetitive surge peak Off-state	$V_{DSM}$	V <sub>DRM</sub> +100	V
Non repetitive peak reverse voltage	$V_{RSM}$	V <sub>RRM</sub> +100	V
RMS on-state current	$I_{T(RMS)}$	8	Α
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I <sub>TSM</sub>	80	Α
I <sup>2</sup> t value for fusing (tp=10ms)	l <sup>2</sup> t	32	A <sup>2</sup> s
Critical rate of rise of on-state current	41/4 <del>+</del>	50	Λ/110
$(I_G=2\times I_{GT})$	dl/dt	50	A/µs
Peak gate current	l <sub>GM</sub>	4	Α
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	$P_GM$	5	W

#### THERMAL RESISTANCES

junction to case(AC)	R <sub>th(i-c)</sub>	2.7	°C/W

BTB08

Rev0\_19012023EBJ







# **ELECTRICAL CHARACTERISTICS at** (Ta = 25 °C Unless otherwise **3 Quadrants**

Parameter	Quadrant	Cumbal	mbol Test Condition		hal Test Condition Min/ Value			Unit	
Parameter	Quadrant	Syllibol	rest Condition	Max	TW	SW	CW	BW	Offic
Gate trigger current	I-II-III	l <sub>GT</sub>	$V_{D} = 12V R_{I} = 33\Omega$	Max	5	10	35	50	mA
Gate trigger voltage	I-II-III	$V_{GT}$	V <sub>D</sub> -12V K <sub>L</sub> -33Ω	Max	1.5				V
Non-triggering gate voltage	I-II-III	$V_{\sf GD}$	$V_D = V_{DRM}Tj = 125$ °C $R_L = 3.3$ K $\Omega$	Min		0	.2		٧
Latching current	I-III	ı	I <sub>G</sub> =1.2I <sub>GT</sub>	Max	20	25	50	70	mA
Laterling current	II	ΙL	IG-1.2IGT	Max	25	35	70	90	ША
Holding current		I <sub>H</sub>	I <sub>T</sub> =100mA	Max	15	20	40	60	mA
Critical rate of decrease commutating on-state		dV/dt	V <sub>D</sub> =2/3V <sub>DRM</sub> Gate Open T <sub>j</sub> =125°C	Min	50	200	500	1000	V/µs

## 4 Quadrants

Parameter	Quadrant	Symbol	Test Condition		Value		Unit	
Farameter	Parameter Quadrant Symbol Test Condition		Max	С	В			
Gate trigger current	I-II-III	_		Max	25	50	mA	
Oate trigger current	IV	I <sub>GT</sub>	$V_{D} = 12V R_{I} = 33\Omega$	IVIAA	50	70	шА	
Gate trigger voltage	ALL	$V_{GT}$	B [ 33		1	.5	V	
Non-triggering gate voltage	ALL	$V_{\sf GD}$	$V_D = V_{DRM} T_j = 125^{\circ}C R_L = 3.3K\Omega$		0.2		٧	
Latching current	I-III-IV	_	1 -1 21		50	70	mA	
Latering current	II	Ι <sub>L</sub>	$I_{G}=1.2I_{GT}$	Max	70	90	IIIA	
Holding current		I <sub>H</sub>	I <sub>T</sub> =200mA	MAX	40	60	mA	
Critical rate of decreas		dV/dt	$V_D$ =2/3 $VD_{RM}$ Gate Open $T_i$ =125°C	MIN	200	500	V/µs	

## STATIC CHARACTERISTICS

Parameter		Symbol	Test Condition	Value (Max)	Unit
Peak on-state voltage drop	T <sub>j</sub> =25°C	$V_{TM}$	I <sub>τм</sub> =11A tp=380μs	1.5	V
Maximum forward and reverse leakage	T <sub>j</sub> =25°C	I <sub>DRM</sub>	\\ -\\ \\ \\ -\\	5	μA
Maximum leakage current for diodes	T <sub>j</sub> =125°C	I <sub>RRM</sub>	$V_D = V_{DRM} V_R = V_{RRM}$	1	mA





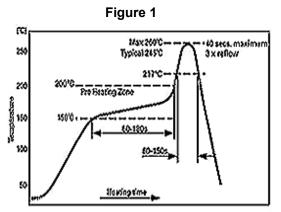


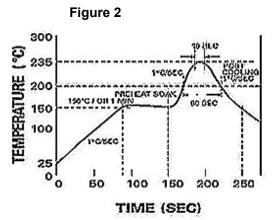
#### **Recommended Reflow Solder Profiles**

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.





## Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat  – Temperature Range  – Time	150-170°C 60-180 seconds	150-200°C 60-180 seconds
Time maintained above:  – Temperature  – Time	200°C 30-50 seconds	217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.





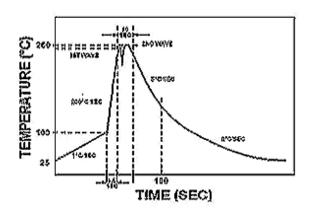


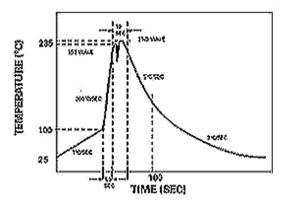
An IATF 16949, ISO9001 and ISO 14001/ISO 45001 Certified Company

### **Recommended Wave Solder Profiles**

The Recommended solder Profile For Devices
with Pb-free terminal plating where a Pb-free solder is used

The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder





## **Wave Profiles in Tabular Form**

Profile Feature	Sn-Pb System	Pb-free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.







## **TYPICAL CHARACTERISTIC CURVES**

Fig 1: Maximum power dissipation versus RMS on-state current

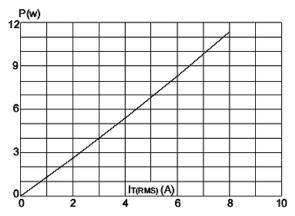


Fig 2: Surge peak on-state current versus number of cycles

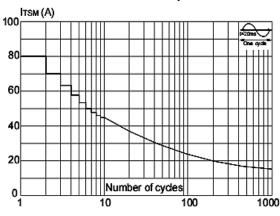


Fig 3: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I t (dl/dt < 50A/μs)

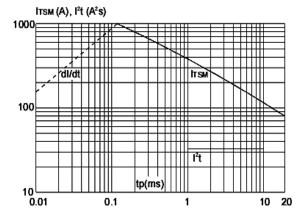


Fig 4: RMS on-state current versus case temperature

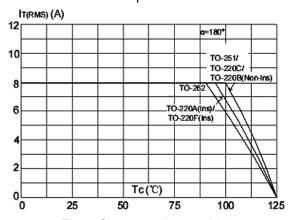


Fig 5: On-state characteristics (maximum values)

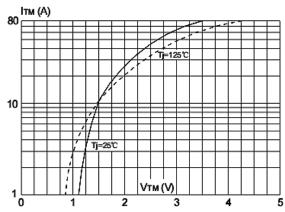
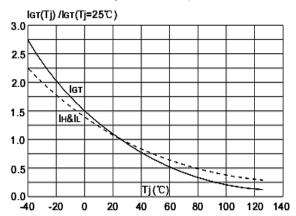


Fig 6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



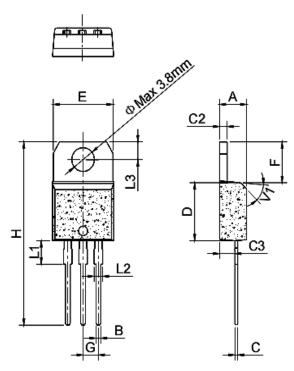






## **PACKAGE DETAILS**

TO-220 Leaded Plastic Package



	Dimensions						
Ref.	М	illimet		Inches			
	Min	Тур	Max	Min	Тур	Max	
Α	4.40		4.60	0.173		0.181	
В	0.61		0.88	0.02		0.035	
С	0.46		0.70	0.02		0.028	
C2	1.21		1.32	0.05		0.052	
C3	2.40		2.72	0.09		0.107	
D	8.60		9.70	0.34		0.382	
Е	9.80		10.4	0.39		0.409	
F	6.55		6.95	0.26		0.274	
G		2.54			0.1		
Н	28.0		29.80	1.1		1.173	
L		3.75			0.148		
L2	1.14		1.70	0.05		0.067	
L3	2.65		2.95	0.1		0.116	
V1		45°			45°	·	

## **Pin Configuration**

- 1. Terminal 1
- 2. Terminal 2
- 3. Gate







# Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- · Temperature 5 °C to 30 °C
- · Humidity between 40 to 70 %RH
- · Air should be clean.
- · Avoid harmful gas or dust.
- · Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- · Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- · Avoid rapid change of temperature.
- · Avoid condensation.
- · Mechanical stress such as vibration and impact shall be avoided.
- · The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

## **Shelf Life of CDIL Products**

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

## Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

	JEDEC MSL Level						
Level	Time	Condition					
1	Unlimited	≤30 °C / 85% RH					
2	1 Year	≤30 °C / 60% RH					
2a	4 Weeks	≤30 °C / 60% RH					
3	168 Hours	≤30 °C / 60% RH					
4	72 Hours	≤30 °C / 60% RH					
5	48 Hours	≤30 °C / 60% RH					
5a	24 Hours	≤30 °C / 60% RH					
6	Time on Label(TOL)	≤30 °C / 60% RH					





## **Customer Notes**

## **Component Disposal Instructions**

- 1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
- 2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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