6 Amp TRIACs

BTA06 (Insulated)
BTB06 (Non-Insulated)

TO-220

TO-220
Plastic Package
RoHS compliant

GENERAL DISCRIPTION :

With high ability to withstand the shock loading of large current, BTA06 series triacs provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, the products especially recommended for use on inductive load. From all three terminals to external heatsink, BTB06 provides a rated insulation voltage of 2500 V_{RMS}, and BTA06 provides a rated insulation voltage of 2000 V_{RMS}, complying with UL standards (File ref: E252906). All the packages listed are RoHS compliant. (2011/65/EU)

FEATURES:

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	6	A
V_{DRM} /V_{RRM}	600/800	V

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		T_{stg}	-40 ~ 150	°C
Operating junction temperature range		T_j	-40 ~ 125	°C
Repetitive peak off-state voltage (Tj=25°C)		V_{DRM}	600/800	V
Repetitive peak reverse voltage (Tj=25°C)		V_{RRM}	600/800	
RMS on-state current	Insulated (T_C=100°C)	$I_{T(RMS)}$	6	A
	Non-Insulated (T_C=105°C)			
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	60	A
I^2t value for fusing (tp=10ms)		I^2t	18	A^2s
Critical rate of rise of on-state current (I_G=2×I_{GT})	I-II-III	dI/dt	50	A/µs
	IV		10	
Peak gate current		I_{GM}	2	A
Average gate power dissipation		$P_{G(AV)}$	1	W
Peak gate power		P_{GM}	5	W

THERMAL RESISTANCES

PARAMETER		SYMBOL	VALUE	UNIT
Junction to case(AC)	Insulated	$R_{th(j-c)}$	2.9	°C/W
	Non-Insulated		2.3	

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ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

3 Quadrants

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION		VALUE				UNIT
					TW	SW	CW	BW	
Gate Trigger Current	I_{GT}	I-II-III	V_D =12V R_L =30Ω	MAX	5	10	35	50	mA
Gate Trigger Voltage	V_{GT}	I-II-III			1.5				V
Off-State Gate Voltage	V_{GD}	I-II-III	V_D =V_{DRM} T_j =125°C R_L =3.3KΩ	MIN	0.2				V
Latching Current	I_L	I-III	I_G =1.2I_{GT}	MAX	10	15	50	70	mA
		II			15	25	60	80	
Holding Current	I_H	I_T =0.2A		MAX	6	10	35	60	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	V_D=2/3V_{DRM} Gate Open T_j =125°C		MIN	50	100	400	1000	V/μs
Critical rate of decrease of commutating on-state current	(dI/dt)c	Without sunbber T_j =125°C		MIN	1.2	2.4	3.5	5.3	A/ms

4 Quadrants

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION		VALUE		UNIT
					C	B	
Gate Trigger Current	I_{GT}	I - II - III	V_D =12V R_L =30Ω	MAX	25	50	mA
		IV		MAX	50	70	
Gate Trigger Voltage	V_{GT}	ALL		MAX	1.5		V
Off-State Gate Voltage	V_{GD}	ALL	V_D =V_{DRM} T_j =125°C R_L=3.3KΩ	MIN	0.2		V
Latching Current	I_L	I - III	I_G =1.2I_{GT}	MAX	50	70	mA
		II		MAX	60	80	
Holding Current	I_H	I_T =0.2A		MAX	40	60	mA
Critical Rate of Rise of Off-State Voltage	dV/dt	VD=2/3V_{DRM} Gate Open T_j=125°C		MIN	200	500	V/μs

STATIC CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITION	VALUE (MAX)	UNIT
On-State Voltage	T_j=25°C	V_{TM}	I_{TM} =8.5A t_p=380μs	1.5	V
Off-State Leakage Current	T_j=25°C	I_{DRM}	V_D =V_{DRM} , V_R =V_{RRM}	5	μA
	T_j=125°C	I_{RRM}		1	mA

TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum power dissipation versus RMS on-state current

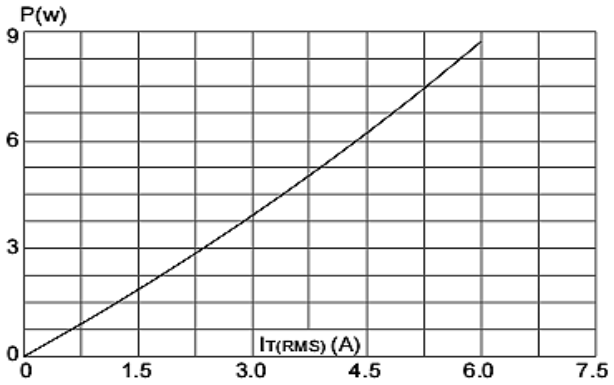


Fig 2: Surge peak on-state current versus number of cycles

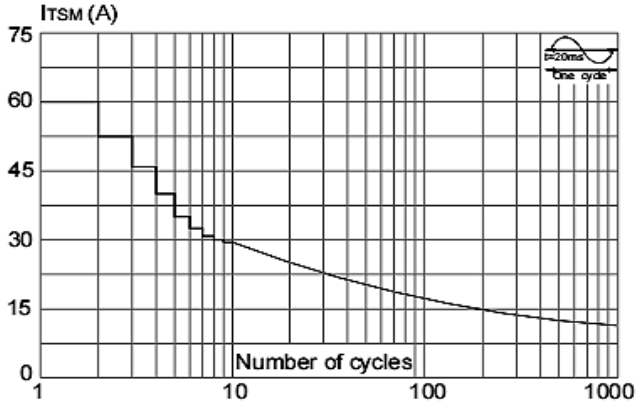


Fig 3: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I t (I-II-III:dI/dt < 50A/µs; IV:dI/dt < 10A/µs)

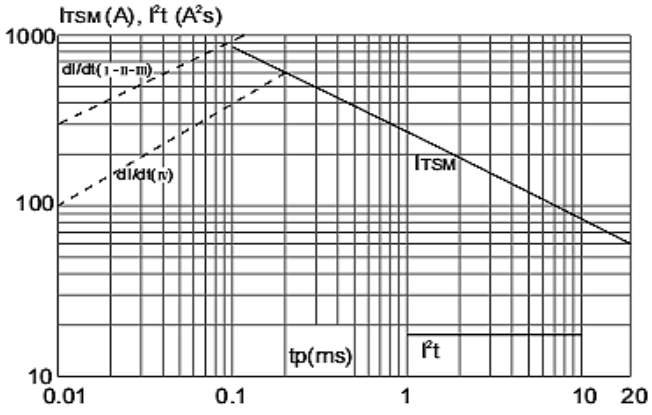


Fig 4: RMS on-state current versus case temperature

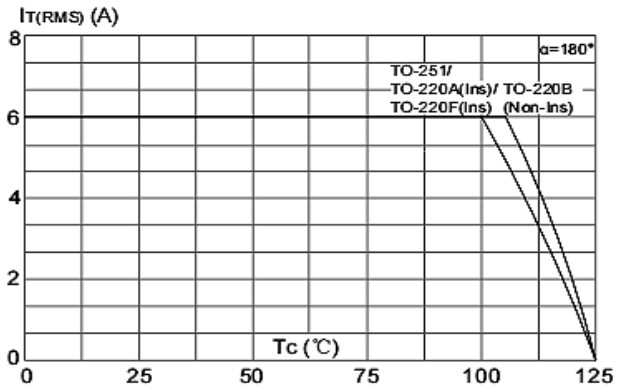


Fig 5: On-state characteristics (maximum values)

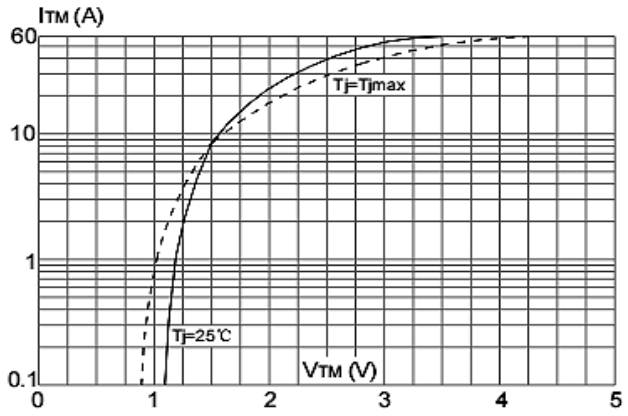
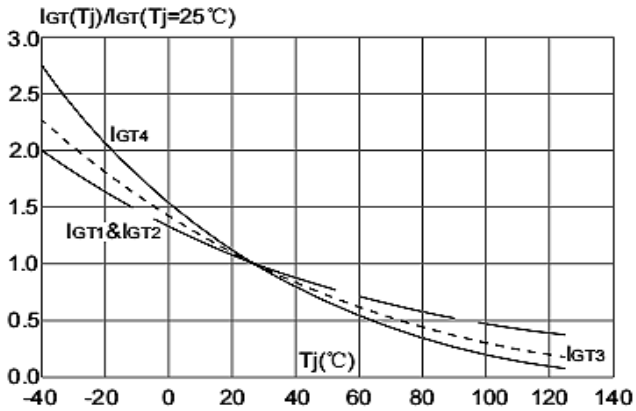


Fig 6: Relative variations of gate trigger current versus junction temperature



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TYPICAL CHARACTERISTICS CURVES

Fig 7: Relative variations of holding current versus junction temperature

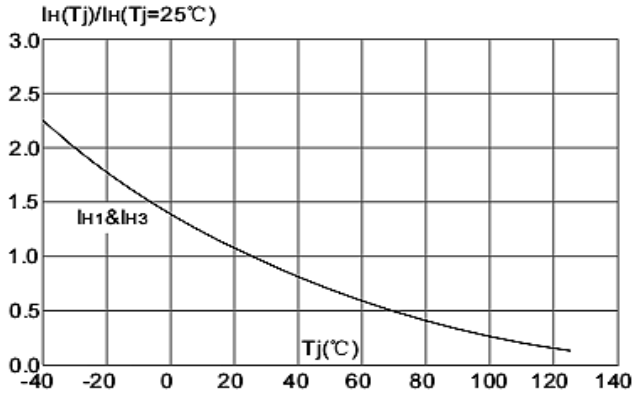
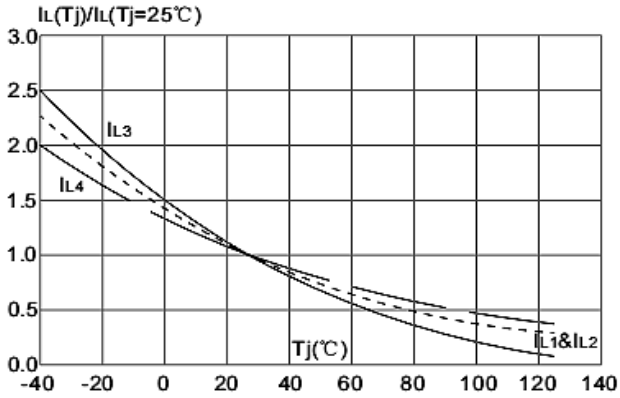
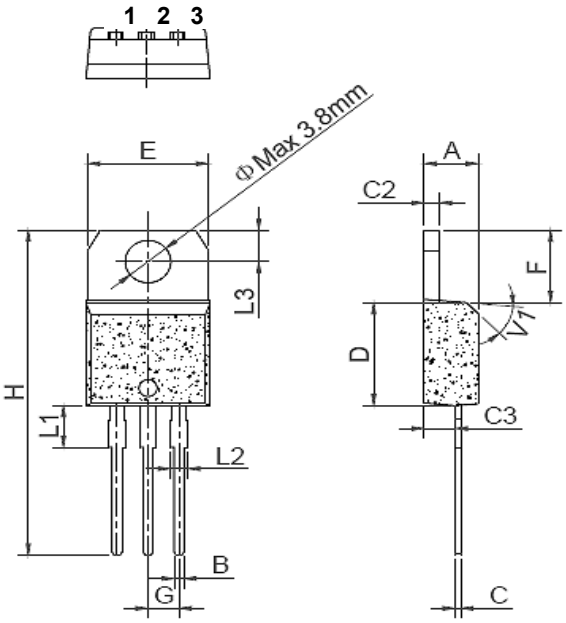


Fig 8: Relative variations of latching current versus junction temperature



PACKAGE DETAILS

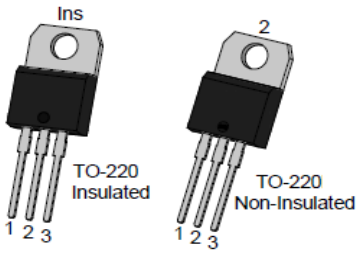
TO-220 Insulated/ Non-insulated Leaded Plastic Package



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.17		0.18
B	0.61		0.88	0.02		0.04
C	0.46		0.70	0.02		0.03
C2	1.21		1.32	0.05		0.05
C3	2.40		2.72	0.09		0.11
D	8.60		9.70	0.34		0.38
E	9.80		10.4	0.39		0.41
F	6.55		6.95	0.26		0.27
G		2.54			0.1	
H	28.0		29.8	1.1		1.17
L1		3.75			0.15	
L2	1.14		1.70	0.05		0.07
L3	2.65		2.95	0.1		0.12
V1		45°			45°	

Pin Configuration

1. T1
2. T2
3. Gate



ORDERING INFORMATION

BT	X	6	-XXX	XX
TRIAC	A: Insulated B: Non-insulated	$I_{T(RMS)}$ 6A	600: V_{DRM}/V_{RRM} 800: V_{DRM}/V_{RRM}	TW: I_{GT1-3}≤5mA SW: I_{GT1-3}≤10mA CW: I_{GT1-3}≤35mA BW: I_{GT1-3}≤50mA C: I_{GT1-3}≤25mA I_{GT4}≤50mA B: I_{GT1-3}≤50mA I_{GT4}≤70mA

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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