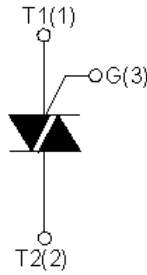
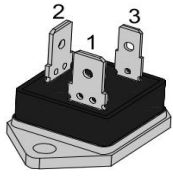


40A TRIACS



BTA40_
TG-C
PLASTIC PACKAGE

With high ability to withstand the shock loading of large current, BTA40 series triacs provide high dv/dt rate with strong resistance to electromagnetic interference. With high commutation performances, 3 quadrant products especially recommended for use on inductive load.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Storage junction temperature range	T_{stg}	-40 to 150	°C
Operating junction temperature range	T_j	-40 to 125	°C
Repetitive peak off-state voltage ($T_j = 25^\circ\text{C}$)	V_{DRM}	600/800/1200/1600	V
Repetitive peak reverse voltage ($T_j = 25^\circ\text{C}$)	V_{RRM}	600/800/1200/1600	V
Non repetitive surge peak off-state voltage	V_{DSM}	$V_{DRM} + 100$	V
Non repetitive peak reverse voltage	V_{RSM}	$V_{RRM} + 100$	V
RMS on-state current ($T_c = 90^\circ\text{C}$)	$I_{T(RMS)}$	40	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I_{TSM}	400	A
I^2t value for fusing ($t_p=10\text{ms}$)	I^2t	880	A ² s
Critical rate of rise of on-state current ($I_G = 2 \times I_{GT}$)	dI/dt	50	A/ μs
Peak gate current	I_{GM}	4	A
Average gate power dissipation	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	10	W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

3 Quadrants

Parameter	Test Condition	Symbol		Quadrant	Values	Unit
Gate Trigger Current	$V_D = 12\text{V}, R_L = 33\Omega$	I_{GT}	MAX	I-II-III	50	mA
Gate Trigger Voltage		V_{GT}	MAX	I-II-III	1.3	V
Off-State Gate Voltage	$V_D = V_{DRM}, T_j = 125^\circ\text{C}, R_L = 3.3\text{K}\Omega$	V_{GD}	MIN	I-II-III	0.2	V
Latching Current	$I_G = 1.2 I_{GT}$	I_L	MAX	I-III	80	mA
				II	100	
Holding Current	$I_T = 100\text{mA}$	I_H	MAX		60	mA
Critical Rate of Rise of Off-State Voltage	$V_D = 2/3 V_{DRM}, \text{Gate Open}, T_j = 125^\circ\text{C}$	dV/dt	MIN		1500	V/ μs

4 Quadrants

Parameter	Test Condition	Symbol		Quadrant	Values	Unit
Gate Trigger Current	$V_D = 12V, R_L = 33\Omega$	I_{GT}	MAX	I-II-III	50	mA
Gate Trigger Voltage				IV	70	
Off-State Gate Voltage	$V_D = V_{DRM}, T_J = 125^\circ C, R_L = 3.3K\Omega$	V_{GD}	MIN	I-II-III	0.2	V
Latching Current	$I_G = 1.2 I_{GT}$	I_L	MAX	I-III	90	mA
Holding Current				II	100	
Critical Rate of Rise of Off-State Voltage	$V_D = 2/3 V_{DRM}, \text{Gate Open}, T_J = 125^\circ C$	dV/dt	MIN		1000	V/ μs

Static Characteristics

Parameter	Test Conditions	Symbol		Value	Unit
On-State Voltage	$I_{TM} = 60A, tp = 380\mu s$	V_{TM}	$T_J = 25^\circ C$	1.5	V
Off-State Leakage Current	$V_D = V_{DRM}, V_R = V_{RRM}$	I_{DRM}	$T_J = 25^\circ C$	10	μA
		I_{RRM}	$T_J = 125^\circ C$	5	mA

Thermal Resistance

Parameter	Symbol	Value	Unit
Maximum Thermal Resistance Junction to case (AC)	$R_{th(j-c)}$	0.65	$^\circ C/W$

Device Name	
BTA40 – xxx yy	
xxx	yy
600: $V_{DRM}/V_{RRM} \geq 600V$	BW: $I_{GT I-III} \leq 50mA$
800: $V_{DRM}/V_{RRM} \geq 800V$	
1200: $V_{DRM}/V_{RRM} \geq 1200V$	B: $I_{GT I-III} \leq 50mA, I_{GT IV} \leq 70mA$
1600: $V_{DRM}/V_{RRM} \geq 1600V$	

CHARACTERISTIC CURVES

FIG.1 Maximum power dissipation versus RMS on-state current

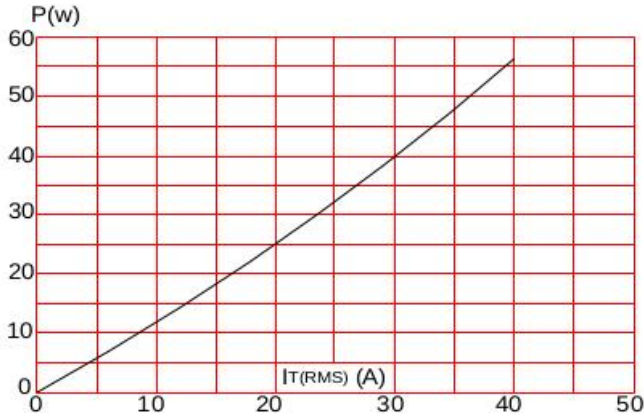


FIG.2: RMS on-state current versus case temperature

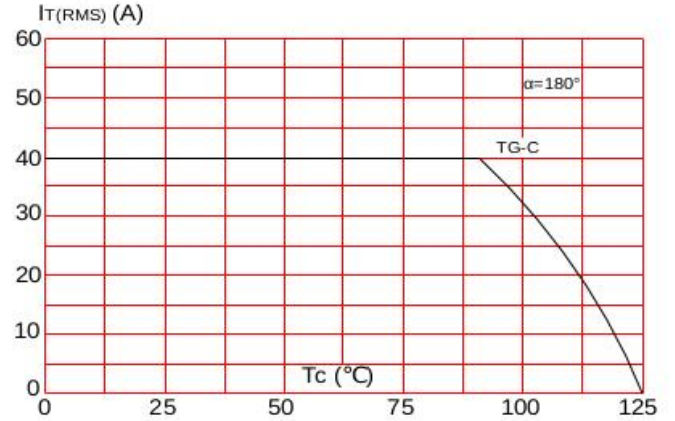


FIG.3: Surge peak on-state current versus number of cycles

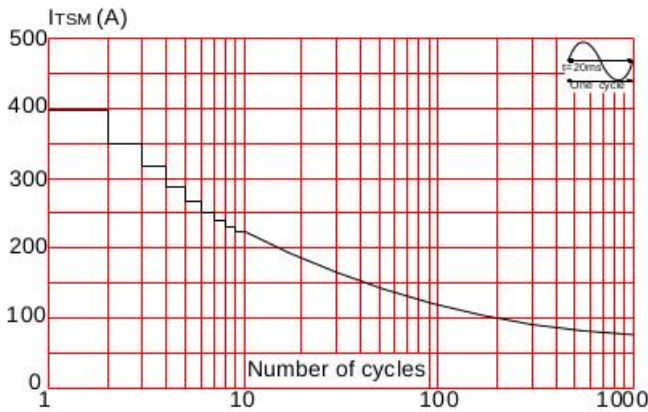


FIG.4: On-state characteristics (maximum values)

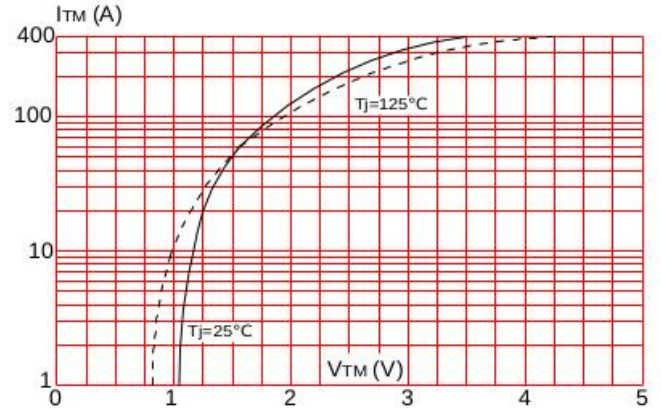


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\mu s$, and corresponding value of I_t ($di/dt < 50A/\mu s$)

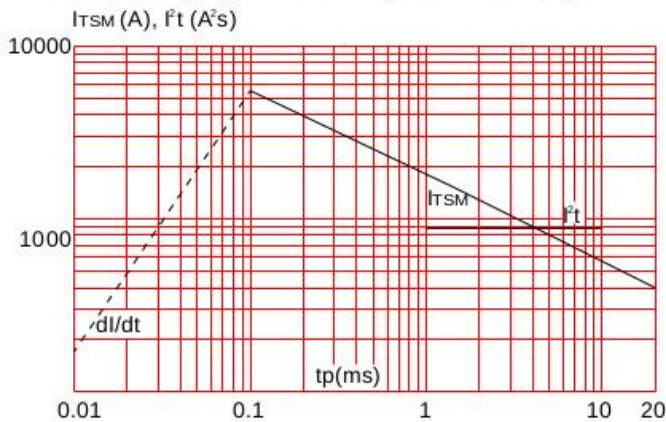
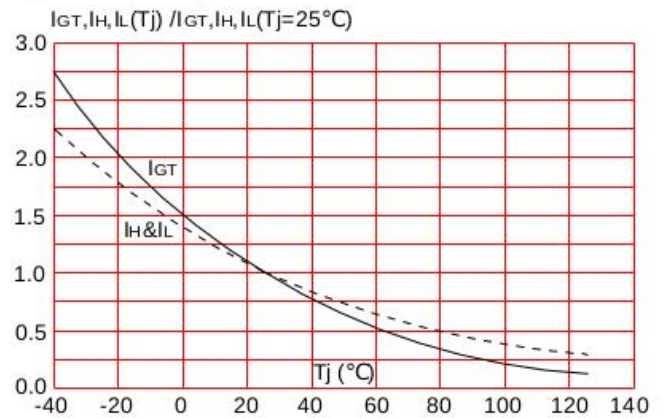
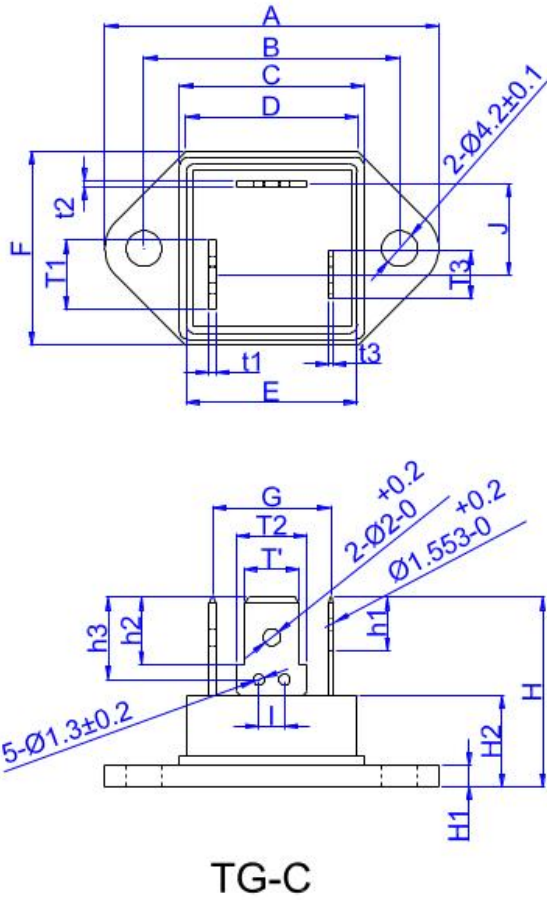


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



PACKAGE OUTLINE AND DIMENSIONS



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			39.2			1.543
B	29.8	30.0	30.2	1.173	1.181	1.189
C			21.6			0.85
D			20.2			0.795
E			20.5			0.791
F			23			0.906
T1, T2		8.10			0.318	
T3		5.65			0.222	
T'		6.35			0.25	
t1, t2		0.8			0.031	
t3		0.6			0.023	
G		13.9			0.547	
H1		2.6			0.102	
H2		10.8			0.425	
H			22.8			0.886
h1	6.2	6.35	6.5	0.244	0.25	0.256
h2	7.8	7.95	8.1	0.307	0.313	0.319
h3	9.45	9.75	10.05	0.372	0.384	0.396
I	2.7	3.0	3.3	0.106	0.118	0.130
J		10.8			0.425	



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Customer Notes:

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

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