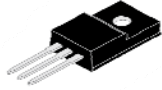
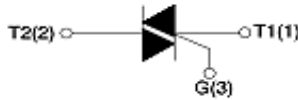


## 25A TRIAC

## BTA24F 600/800/1200



TO-220FP



### TO-220FP

Fully Insulated  
Plastic Package  
RoHS compliant

### General Description:

With high ability to withstand the shock loading of large current, BTA24F series triacs provide high dv/dt rate with strong resistance to electromagnetic interference. With high commutation performances, 3 quadrant products especially recommended for use on inductive load.

### ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage (T <sub>j</sub> =25°C)	V <sub>DRM</sub>	600 / 800 / 1200	V
Repetitive peak reverse voltage (T <sub>j</sub> =25°C)	V <sub>RRM</sub>	600 / 800 / 1200	V
Non repetitive surge peak Off-state voltage	V <sub>DSM</sub>	V <sub>DRM</sub> +100	V
Non repetitive peak reverse voltage	V <sub>RSM</sub>	V <sub>RRM</sub> +100	V
RMS on-state current	I <sub>T(RMS)</sub>	25	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I <sub>TSM</sub>	250	A
I <sup>2</sup> t value for fusing (tp=10ms)	I <sup>2</sup> t	340	A <sup>2</sup> s
Critical rate of rise of on-state current (I <sub>G</sub> = 2×I <sub>GT</sub> )	di/dt	50	A/μs
Peak gate current	I <sub>GM</sub>	4	A
Average gate power dissipation	P <sub>G(AV)</sub>	1	W
Peak gate power	P <sub>GM</sub>	10	W
Storage junction temperature range	T <sub>stg</sub>	-40 to +150	°C
Operating junction temperature range	T <sub>j</sub>	-40 to +125	°C

### THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance junction to case(AC)	Rth(j-c)	1.7	°C/W



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**ELECTRICAL CHARACTERISTICS at** (Ta = 25 °C Unless otherwise specified)

**V<sub>DRM</sub> / V<sub>R RM</sub> : 600/800V**

PARAMETER	QUADRANT	SYMBOL	TEST CONDITION	BTA24F-600/800			UNIT
					BW	CW	
Gate Trigger Current	I-II-III	I <sub>GT</sub>	V <sub>D</sub> =12V, R <sub>L</sub> =33Ω	MAX	50	35	mA
Gate Trigger Voltage	I-II-III	V <sub>GT</sub>		MAX	1.3		V
Non-trigger gate voltage	I-II-III	V <sub>GD</sub>	V <sub>D</sub> =V <sub>DRM</sub> , T <sub>j</sub> =125°C, R <sub>L</sub> =3.3kΩ	MIN	0.2		V
Latching Current	I-III	I <sub>L</sub>	I <sub>G</sub> = 1.2I <sub>GT</sub>	MAX	80	70	mA
	II				100	80	
Holding Current		I <sub>H</sub>	I <sub>T</sub> = 100mA	MAX	75	50	mA
Critical rate of rise of off-state voltage		dV/dt	V <sub>D</sub> =2/3V <sub>DRM</sub> Gate Open, T <sub>j</sub> =125°C	MIN	1000	500	V/μA

**V<sub>DRM</sub> / V<sub>R RM</sub> : 1200V**

PARAMETER	QUADRANT	SYMBOL	TEST CONDITION	BTA24F-1200			UNIT
					BW	CW	
Gate Trigger Current	I-II-III	I <sub>GT</sub>	V <sub>D</sub> =12V, R <sub>L</sub> =33Ω	MAX	50	35	mA
Gate Trigger Voltage	I-II-III	V <sub>GT</sub>		MAX	1.5		V
Non-trigger gate voltage	I-II-III	V <sub>GD</sub>	V <sub>D</sub> =V <sub>DRM</sub> , T <sub>j</sub> =125°C, R <sub>L</sub> =3.3kΩ	MIN	0.2		V
Latching Current	I-III	I <sub>L</sub>	I <sub>G</sub> = 1.2I <sub>GT</sub>	MAX	90	70	mA
	II				100	80	
Holding Current		I <sub>H</sub>	I <sub>T</sub> = 100mA	MAX	80	60	mA
Critical rate of rise of off-state voltage		dV/dt	V <sub>D</sub> =2/3V <sub>DRM</sub> Gate Open, T <sub>j</sub> =125°C	MIN	1500	1000	V/μA

**STATIC CHARACTERISTICS**

PARAMETER		SYMBOL	TEST CONDITION	VALUE	UNIT
Peak on-state voltage drop	T <sub>j</sub> =25°C	V <sub>TM</sub>	I <sub>TM</sub> =35A t <sub>p</sub> =380μs	MAX	1.5 V
Maximum forward leakage current / Maximum reverse leakage current	T <sub>j</sub> =25°C	I <sub>DRM</sub> / I <sub>R RM</sub>	V <sub>D</sub> =V <sub>DRM</sub> V <sub>R</sub> =V <sub>R RM</sub>	MAX	5 μA
	T <sub>j</sub> =125°C			MAX	3 mA

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## TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum power dissipation versus RMS on-state current

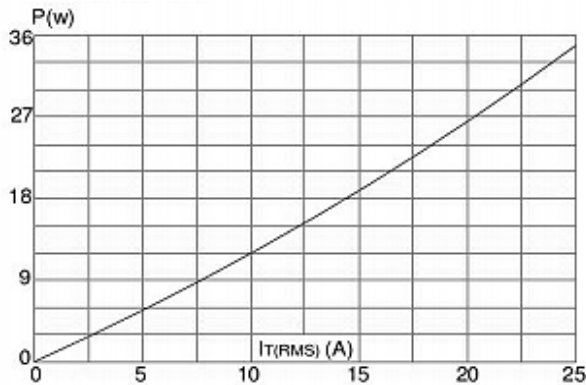


Fig 2: Surge peak on-state current versus number of cycles

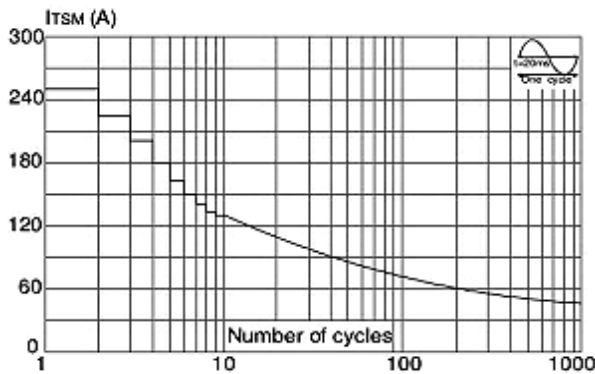


Fig 3: Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10\text{ms}$ , and corresponding value of  $I^2t$  ( $di/dt < 50\text{A}/\mu\text{s}$ )

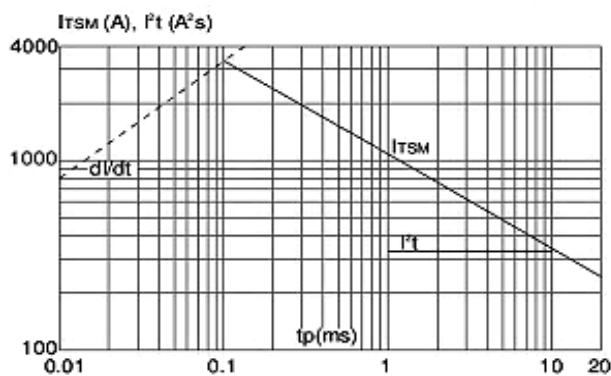


Fig 4: RMS on-state current versus case temperature

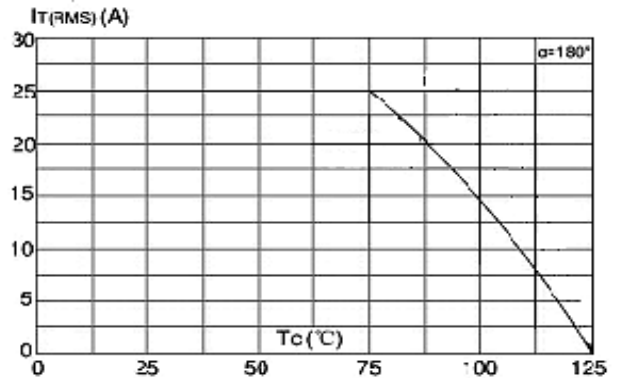


Fig 5: On-state characteristics (maximum values)

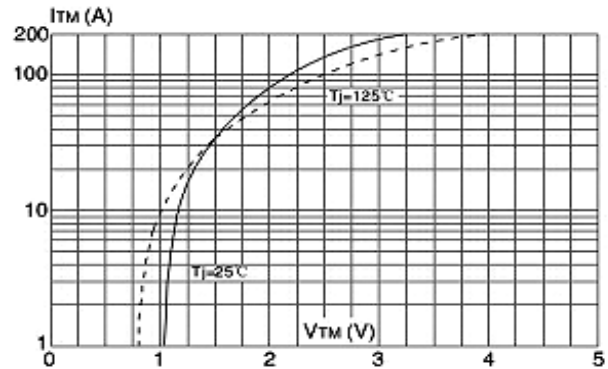
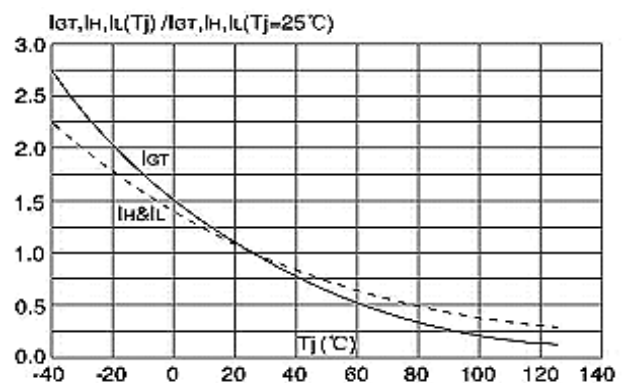
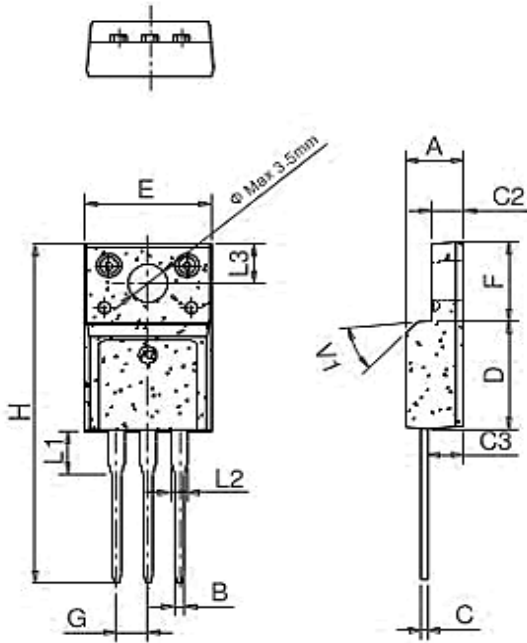


Fig 6: Relative variation of gate trigger current holding current and latching current versus junction temperature



## PACKAGE DETAILS

### TO-220FP PACKAGE OUTLINE AND DIMENSIONS



Ref.	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	4.5		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	



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## Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

### Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

### Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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## Customer Notes

### Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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