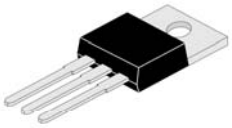
8A TRIACs

BTA08 - 600/800/1200



TO-220 Leaded Insulated Plastic Package
RoHS compliant

TO-220

GENERAL DISCRIPTION:

BTA08 Series Triacs, with high ability to withstand the shock loading of large current, provide high dV/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 Quadrants products especially recommended for use on Inductive Load. It provides Insulation voltage rated at 2500V RMS from all three terminals to external heatsink complying with UL standards.

APPLICATIONS: High commutation performances.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Repetitive Peak Off-State Voltage (Tj=25°C)	V_{DRM}	600/800/1200	V
Repetitive Peak Reverse Voltage (Tj=25°C)	V_{RRM}	600/800/1200	V
Non Repetitive Surge Peak Off-State Voltage	V_{DSM}	VDRM + 100	V
Non Repetitive Peak Reverse Voltage	V_{RSM}	VRRM + 100	V
RMS On-State Current (TC = 100°C)	$I_{T(RMS)}$	8	A
Non Repetitive Surge Peak On-State Current (Full Cycle, f = 50Hz)	I_{TSM}	80	A
I2t Value For Fusing (tp=10ms)	I^2t	32	A^2s
Critical Rate of Rise of On-State Current (IG = 2 X IGT)	dI/dt	50	$A^2\mu s$
Peak Gate Current	I_{GM}	4	A
Average Gate Power Dissipation	$P_{G(AV)}$	1	W
Peak Gate Power	P_{GM}	5	W
Storage Junction Temperature Range	T_{STG}	-40 to +150	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C

Thermal Resistance

PARAMETER	SYMBOL	VALUE	UNIT
Maximum Thermal Resistance Junction to case	$R_{th(j-c)}$	4.0	°C/W

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

3 Quadrants

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION	VALUE				UNIT
				TW	SW	CW	BW	
Gate Trigger Current	I_{GT}	I - II - III	V_D=12V, R_L=33Ω	<5	<10	<35	<50	mA
Gate Trigger Voltage	V_{GT}	I - II - III		<1.5				V
Off-State Gate Voltage	V_{GD}	I - II - III	V_D=V_{DRM}, T_j=125°C, R_L = 3.3KΩ	>0.2				V
Latching Current	I_L	I - III	I_G=1.2 X I_{GT}	<15	<20	<50	<70	mA
		II		<25	<35	<60	<80	
Holding Current	I_H		I_{TM} = 100mA	<10	<15	<40	<60	mA
Critical Rate of Rise of Off-State Voltage	dV/dt		V_D = 2/3 V_{DRM}, Gate Open, T_j=125°C	>50	>200	>500	>1000	V/µs

4 Quadrants

PARAMETER	SYMBOL	QUADRANT	TEST CONDITION	VALUE BTA08		UNIT
				C	B	
Gate Trigger Current	I_{GT}	I - II - III	V_D=12V, R_L=33Ω	<25	<50	mA
		IV		<50	<70	
Gate Trigger Voltage	V_{GT}	ALL		<1.5		V
Off-State Gate Voltage	V_{GD}	ALL	V_D=V_{DRM}, T_j=125°C, R_L = 3.3KΩ	>0.2		V
Latching Current	I_L	I - III - IV	I_G=1.2 X I_{GT}	<35	<50	mA
		II		<60	<80	
Holding Current	I_H		I_T = 200mA	<25	<50	mA
Critical Rate of Rise of Off-State Voltage	dV/dt		V_D = 2/3 V_{DRM}, Gate Open, T_j=125°C	>200	>500	V/µs

STATIC CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITION	VALUE		UNIT
				MIN	MAX	
On-State Voltage	T_J=25°C	V_{TM}	I_{TM}=11A, t_p=380µs	1.55	--	V
Off-State Leakage Current	T_J = 25°C	I_{DRM} / I_{RRM}	V_D = V_{DRM}, V_R = V_{RRM}	5	--	µA
	T_J =125°C			1	--	mA

TYPICAL CHERESTERISTIC CURVES

Fig 1: Maximum power dissipation versus RMS On-State current

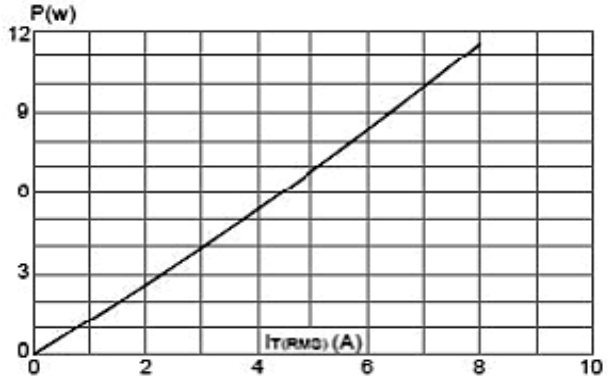


Fig 2: RMS On-State current versus case Temperature

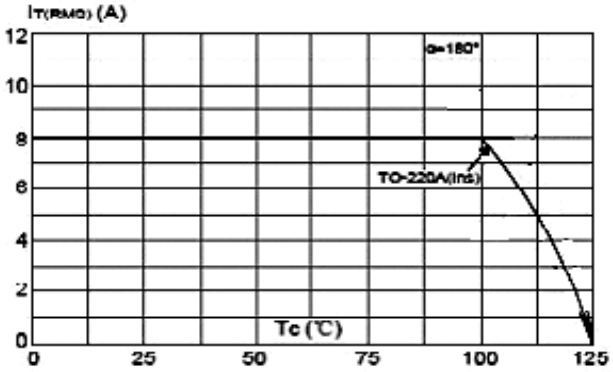


Fig 3: Surge peak On-State current versus number of cycles

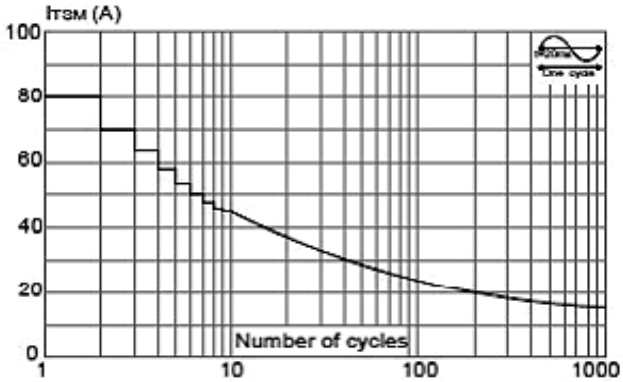


Fig 4: On-State characteristics (maximum value)

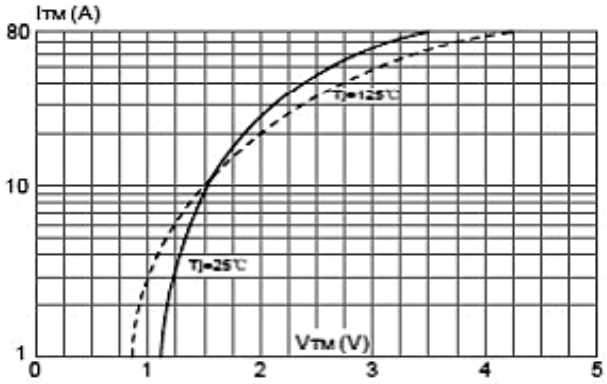


Fig 5: Non-Repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I^2t (dI/dt<50A/us)

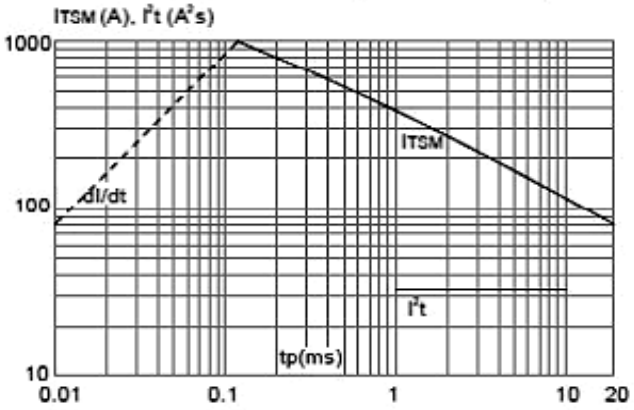
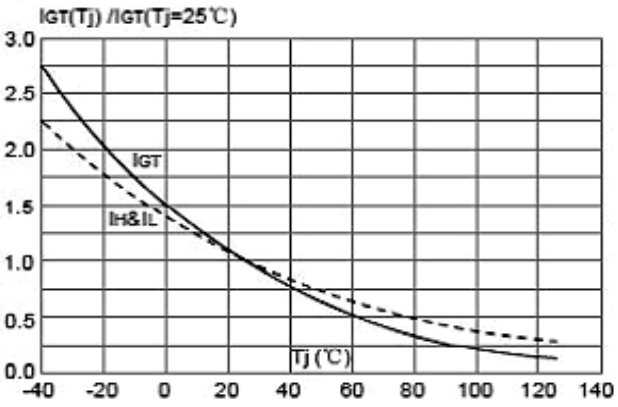
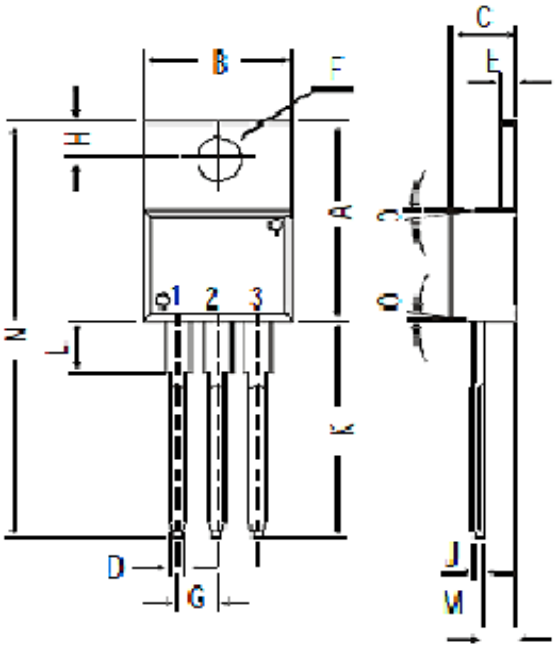


Fig 6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



PACKAGE DETAILS

TO-220 (INSULATED) PACKAGE OUTLINE AND DIMENSION



All dimensions in mm.

DIM	MIN.	MAX.
A	14.42	16.51
B	9.63	10.67
C	3.56	4.83
D		0.90
E	1.15	1.40
F	3.75	3.88
G	2.29	2.79
H	2.54	3.43
J		0.56
K	12.70	14.73
L	2.80	4.07
M	2.03	2.92
N		31.24
Q	DEG 7	

PIN CONFIGURATION

1. MAIN TERMINAL T1
2. MAIN TERMINAL T2
3. GATE

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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