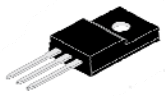
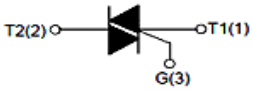
12A TRIAC

BT138X 600/800



TO-220FP



TO-220FP
Fully Isolated
Plastic Package
RoHS compliant

GENERAL DESCRIPTION:

BT138 series triacs with low holding and latching current are especially recommended for use on middle and small resistance type power load.
BT138F provides insulation voltage rated at 2000V.RMS from all three terminals to external heat sink complying with UL standards (File ref: E252906).

FEATURES:

PARAMETER	SYMBOL	VALUE	UNIT
RMS on-state current	$T_{(RMS)}$	12	A
Non repetitive surge peak Off-state voltage/ Repetitive peak reverse voltage(Tj=25℃)	V_{DRM} /$_{VRRM}$	600/800	V

Note: 1.This Product is available in AEC-Q101 Complaint also.
2. For AECQ compliant product, please suffix-AH in the part number while ordering

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER		SYMBOL	VALUE	UNIT
Storage junction temperature range		T_{stg}	-40 -150	°C
Operating junction temperature range		T_j	-40 -125	°C
Repetitive peak off-state voltage(Tj=25°C)		V_{DRM}	600/800	V
Repetitive peak reverse voltage(Tj=25°C)		V_{RRM}	600/800	V
Non repetitive surge peak Off-state voltage		V_{DSM}	VDRM+100	V
Non repetitive peak reverse voltage		V_{RSM}	VRRM+100	V
RMS on-state current	TO-220F(Ins) (T_C=80°C)	$I_{T(RMS)}$	12	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	95	A
I^2t value for fusing (tp=10ms)		I^2t	45	A^2s
Critical rate of rise of on state current(IG=2×IGT)	I-II-III	dI/dt	50	A/µs
	IV		10	
Peak gate current		I_{GM}	2	A
Average gate power dissipation		$P_{G(AV)}$	0.5	W
Average gate power dissipation		P_{GM}	5	W

ELECTRICAL CHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	Quadrant	VALUE			UNIT
				D	E	F	
Triggering gate current	$I_{GT\ (Max)}$	V_D=12V R_L=33Ω	I-II-III	5	10	25	mA
			IV	10	25	70	
Triggering gate voltage	$V_{GT\ (Max)}$		ALL	1.5			V
Non-triggering gate voltage	$V_{GD\ (Min)}$	V_D=V_{DRM}, T_j=125°C, R_L=3 3KΩ	ALL	0.2			V
Latching current	$I_{L\ (Max)}$	I_G=1.2IGT	I- III	15	30	40	mA
			II- IV	20	40	80	
Holding current	$I_{H\ (Max)}$	I_T=100mA	ALL	10	25	30	mA
Critical rate of rise of off-state voltage	dV/dt	V_D=2/3V_{DRM} Gate Open T_j=125°C		20	50	50	V/µs

STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Temp.	Value (Max)	UNIT
Peak on-state voltage drop	V_{TM}	I_{TM}=15A t_p=380µs	Tj=25°C	16	V
Max. Forward Current	I_{DRM}	V_D=V_{DRM} V_R=V_{RRM}	T_j=25°C	5	µA
Max. Reverse Current	I_{RRM}		Tj=125°C	1	mA

THERMAL RESISTANCES

PARAMETER	SYMBOL	TEST CONDITION	Value (Max)	UNIT
Junction to case thermal resistance	$R_{th(j-c)}$	Junction to case(AC)	2.5	°C/W

TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum Power dissipation versus RMS on-state current

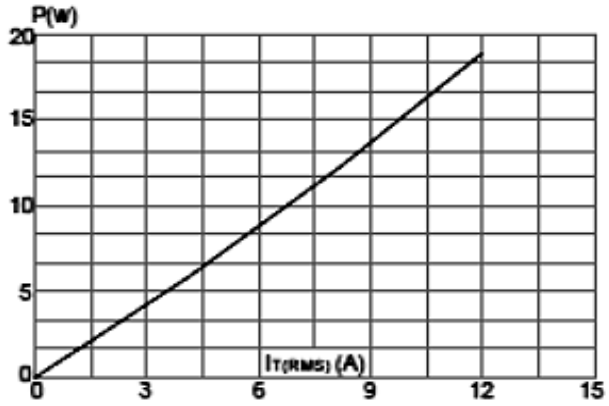


Fig 2: RMS on-state current versus case temperature

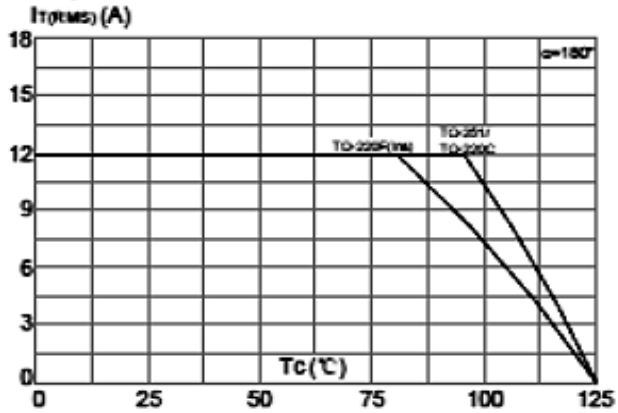


Fig 3: Surge peak on-state current versus number of cycles

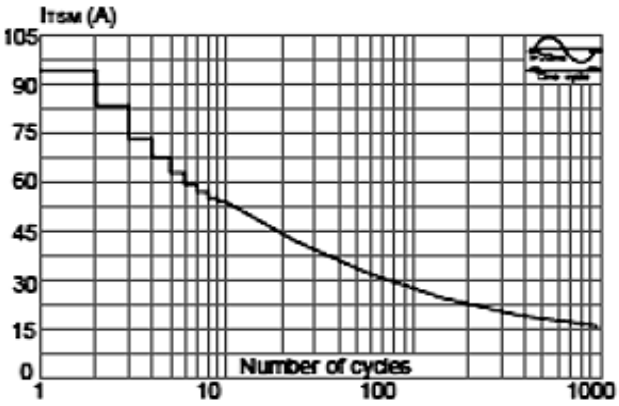
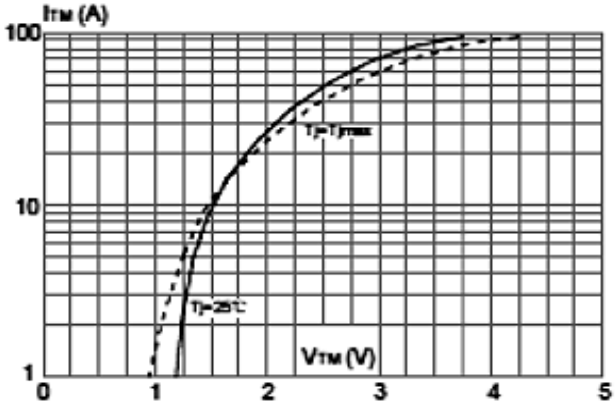


Fig 4: on-state characteristics (maximum value)



TYPICAL CHARACTERISTICS CURVES

Fig 5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I^2t (I-II-III:dI/dt<50A/µs;IV:dI/dt<10A/µs)

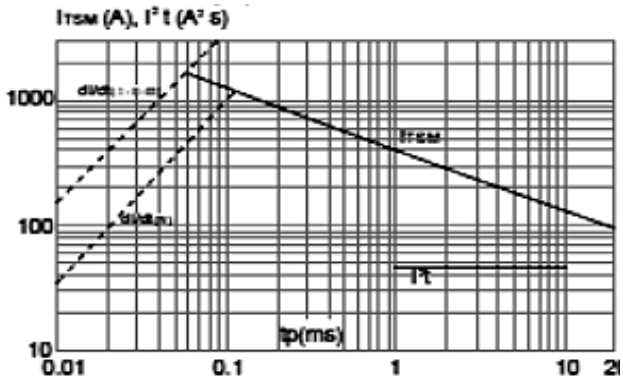


Fig 6: Relative variations of gate trigger current versus junction temperature

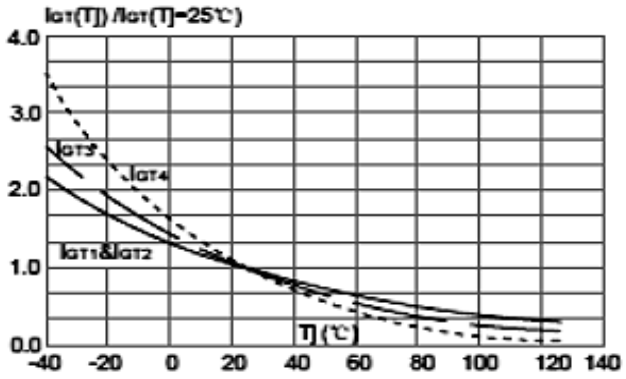


Fig 7: Relative variations of holding current versus junction temperature

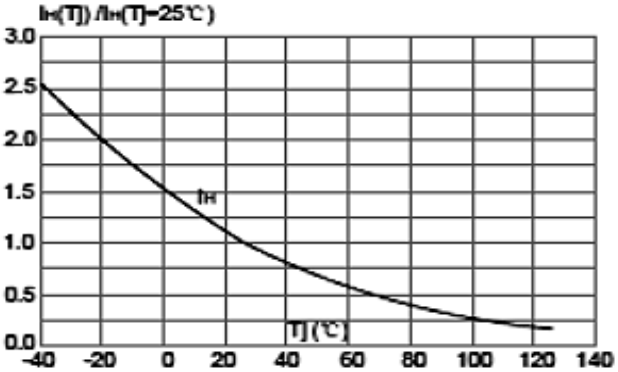
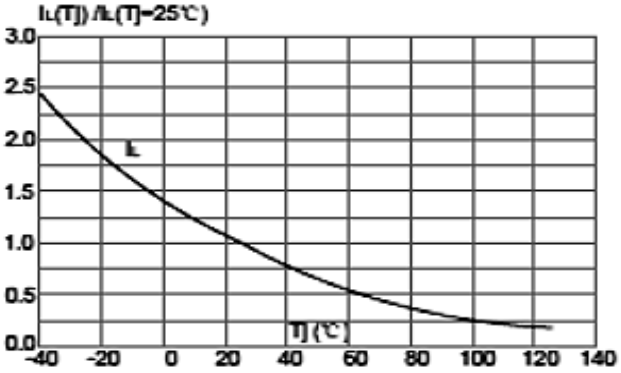
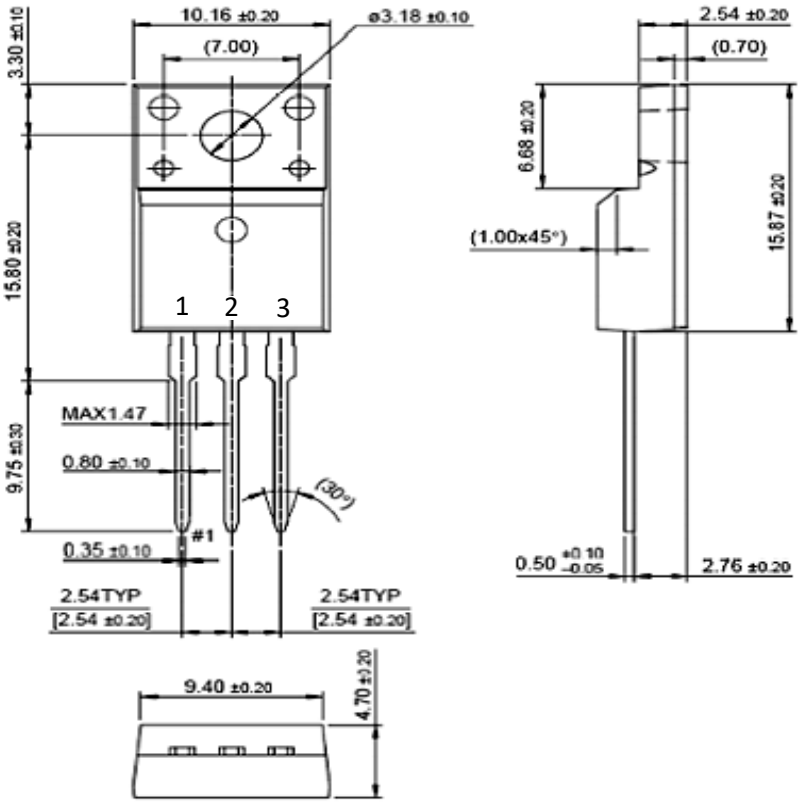


Fig 8: Relative variations of latching current versus junction temperature



PACKAGE DETAILS

TO-220FP Plastic Package



PIN CONFIGURATION

1. Main terminal 1
2. Main terminal 2
3. Gate

PACKAGE	OUTLINE	TUBE (PCS)	INNER BOX (PCS)	PER CARTON
TO-220FP	TUBE	50	1,000	8,000

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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