



4Q 12Amp TRIAC

BT138-600/800



TO-220 Leaded Plastic Package RoHS compliant

TO-220

FEATURE:

- 1. High blocking voltage capability
- 2. Less sensitive gate for improved noise immunity
- 3. Planar passivated for voltage ruggedness and reliability
- 4. Triggering in all four quadrants

APPLICATIONS:

- 1. General purpose motor control
- 2. General purpose switching

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE	UNIT
Peak repetitive off-stage voltage	V_{DRM}, V_{RRM}		600/800	V
On-state RMS current	I _{T(RMS)}	T _L 66°C	12	Α
NON repetitive surge peak on-state current	I _{TSM}	T _p =20ms, T _j =25 °C	95	А
Critical rate of rise on-state current	dI/dt (Q ₁₋₃)	I_{TM} =20A, T_{G} =0.2A	50	A/µs
Peak gate current	I _{GM}		2	Α
Average gate power dissipation	$P_{G(AV)}$		0.5	W
Storage temperature range	T _{stg}		-40 to +150	°C
Operating junction temperature range	T _j		125	°C







ELECTRICALCHARACTERISTICS at (Ta = 25 °C Unless otherwise specified)

DADAMETER	CVMDOL	TEST CONDITION	VALUE			
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
		$T2+G+V_D=12V, I_T=0.1A$			25	mA
Gate trigger current		T2+G- V _D =12V, I _T =0.1A			25	mA
	I _{GT}	T2-G- V _D =12V, I _T =0.1A			25	mA
		T2-G+ V _D =12V, I _T =0.1A			70	mA
Gate trigger voltage	V_{GT}	V _D =12V, I _T =0.1A			1.5	V
Hold current	I _H	V _D =12V, I _T =0.1A			30	mA
Critical rate of rise off-state voltage	dv/dt	$V_D = 67\%V_{DRM}$	50			V/µs
On-state voltage	V_{TM}	I _T =15A			1.65	V
Off-state leakage current	I _{DRM}	$V_D = V_{DRM}$; $T_j = 125$ °C			0.5	mA
Thermal resistance	$R_{th(j-a)}$			60		°C/W
THEITIAL LESISTATICE	R _{th(j-c)}				2.0	C/VV







TYPICAL CHARACTERISTICS CURVES

Fig 1: RMS on-state current as a function of mounting base temperature; maximum values

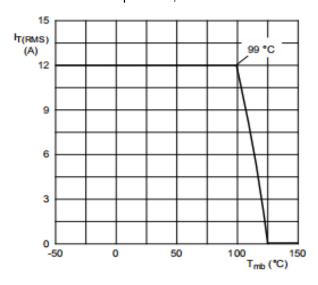


Fig 2: RMS on-state current as a function of surge duration; maximum values

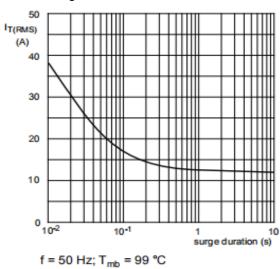
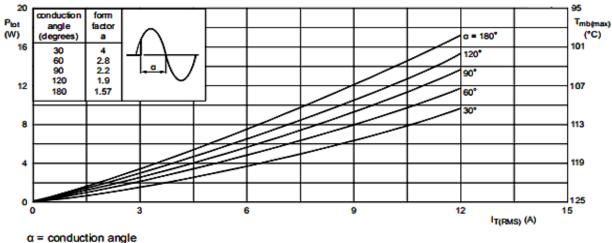


Fig 3: Total power dissipation as a function of RMS on-state current; maximum values



 $a = form factor = I_{T(RMS)} / I_{T(AV)}$



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TYPICAL CHARACTERISTICS CURVES

Fig 4: Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

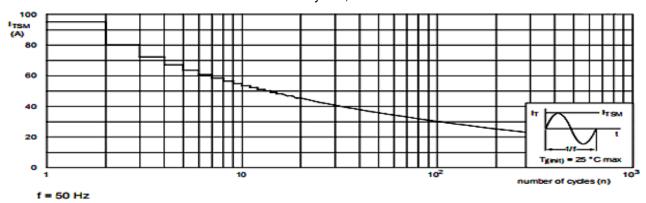
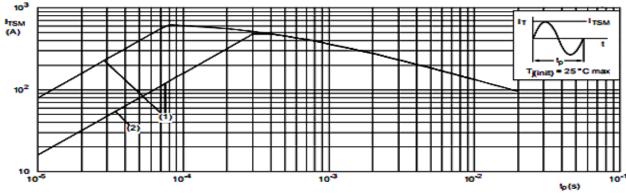


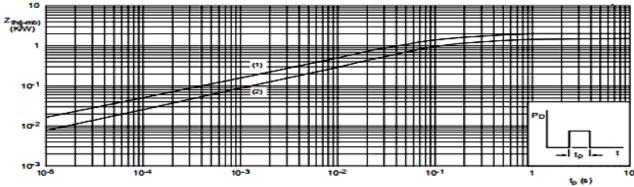
Fig 5: Non-repetitive peak on-state current as a function of pulse width; maximum values



t_o ≤ 20 ms

- (1) dl_T/dt limit
- (2) T2- G+ quadrant limit

Fig 6: Transient thermal impedance from junction to mounting base as a function of pulse duration



- (1) Unidirectional (half cycle)
- (2) Bidirectional (full cycle)

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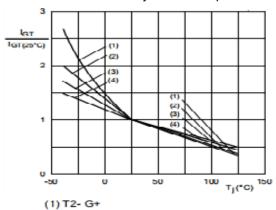


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TYPICAL CHARACTERISTICS CURVES

Fig 7: Normalized gate trigger current as a function of junction temperature



- (2) T2- G-(3) T2+ G-
- (4) T2+ G+
 - Fig 9: Normalized holding current as a function of junction temperature

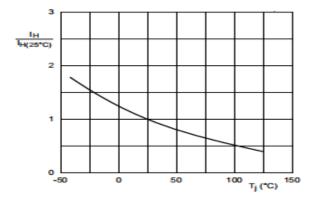


Fig 11: Normalized gate trigger voltage as a function of junction temperature

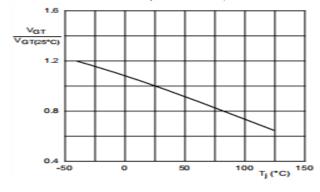


Fig 8: Normalized latching current as a function of junction temperature

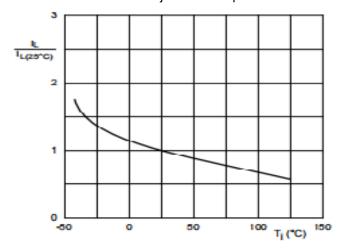
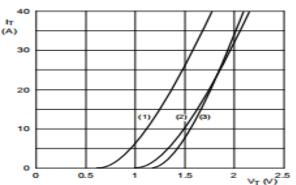


Fig 10: On-state current as a function of on-state voltage



 $V_o = 1.175 \text{ V}; R_s = 0.0316 \Omega$

(1) T_j = 125 °C; typical values

(2) T_i = 125 °C; maximum values

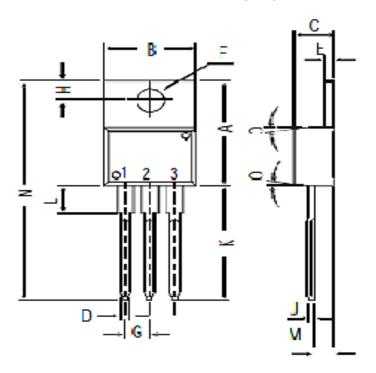
(3) T_j = 25 °C; maximum values





PACKAGE DETAILS

TO-220 Leaded Plastic Package

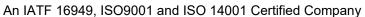


	DIM	MIN.	MAX.	
'n.	A	14.42	16.51	
	В	9.63	10.67	
	С	3.56	4.83	
	D		0.90	
	E	1.15	1.40	
	F	3.75	3.88	
	G	2.29	2.79	
	H	2.54	3.43	
	J		0.56	
E E	K	12.70	14.73	
3	L	2.80	4.07	
ns ons 1	M	2.03	2.92	
≣	N		31.24	
₹	0	DEG 7		

PIN CONFIGURATION

- 1. MAIN TERMINAL T1
- 2. MAIN TERMINAL T2
- 3. GATE







Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- · Temperature 5 °C to 30 °C
- · Humidity between 40 to 70 %RH
- · Air should be clean.
- · Avoid harmful gas or dust.
- · Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- · Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- · Avoid rapid change of temperature.
- · Avoid condensation.
- · Mechanical stress such as vibration and impact shall be avoided.
- · The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level				
Level	Time	Condition		
1	Unlimited	≤30 °C / 85% RH		
2	1 Year	≤30 °C / 60% RH		
2a	4 Weeks	≤30 °C / 60% RH		
3	168 Hours	≤30 °C / 60% RH		
4	72 Hours	≤30 °C / 60% RH		
5	48 Hours	≤30 °C / 60% RH		
5a	24 Hours	≤30 °C / 60% RH		
6	Time on Label(TOL)	≤30 °C / 60% RH		

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Customer Notes

Component Disposal Instructions

- 1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
- 2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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