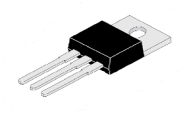
8A TRIAC

BT137-600D/800D



TO-220

TO-220 Leaded
Plastic Package
RoHS compliant

GENERAL DISCRIPTION :

Glass passivated triacs in a plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

FEATURES:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.
Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

PARAMETER	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltages	V_{DRM}	600/800	V
RMS on-state current	$I_{T(RMS)}$	8	A
Non-repetitive peak on-state current	I_{TSM}	85	A

Applications: General Purpose Bidirectional Switching and Phase Control Applications

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE	UNIT
Repetitive peak off-state voltages	V_{DRM}		600/800[1]	V
RMS on-state current	$I_{T(RMS)}$	full sine wave; Tmb ≤ 102 ˚C	8	A
Non-repetitive peak on-state current	I_{TSM}	Full sine wave; Tj= 25˚C prior to surge		
		t = 20ms	65	A
		t = 16.7ms	71	A
I^2t for fusing	I^2t	t = 10ms	21	A^2s
Repetitive rate of rise of on-state current after triggering	dI_T/dt	I_{TM}=12A; I_G=0.2A;dI_G/dt = 0.2A/μs		
		T2+ G+	50	A/μS
		T2+ G-	50	A/μS
		T2- G-	50	A/μS
		T2- G+	10	A/μS
Peak gate current	I_{GM}		2	A
Peak gate voltage	V_{GM}		5	V
Peak gate power	P_{GM}		5	W
Average gate power	$P_{G(AV)}$	Over any 20 ms period	0.5	W
Storage temperature	T_{stg}		-40 ~ 150	°C
Operating junction temperature	T_j		125	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Thermal resistance junction to mounting base	$R_{th\ j\text{-}mb}$	full cycle	--	--	2.0	K/W
		half cycle	--	--	2.4	
Thermal resistance junction to ambient	$R_{th\ j\text{-}a}$	in free air	--	60	--	

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
Gate trigger current	I_{GT}	V_D = 12V; I_T = 0.1A				
		T2+ G+	--	5	35	mA
		T2+ G-	--	8	35	mA
		T2- G-	--	11	35	mA
		T2- G+	--	30	70	mA
Latching current	I_L	V_D = 12V; I_{GT} = 0.1A				
		T2+ G+	--	7	30	mA
		T2+ G-	--	16	45	mA
		T2- G-	--	5	30	mA
		T2- G+	--	7	45	mA
Holding current	I_H	V_D = 12V; I_{GT} = 0.1A	--	5	20	mA
On-state voltage	V_T	I_T = 10A	--	1.3	1.65	V
Gate trigger voltage	V_{GT}	V_D = 12V; I_T = 0.1A	--	0.7	1.5	V
		V_D = 400V; I_T = 0.1A; T_j = 125˚C	0.25	0.4	--	V
Off-state leakage current	I_D	V_D = $V_{DRM(max)}$; T_j = 125˚C	--	0.1	0.5	mA
DYNAMIC CHARACTERISTICS						
Critical rate of rise of off-state voltage	dV_D/dt	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	100	250	--	V/µs
Critical rate of change of commutating voltage	dV_{com}/dt	V_{DM} = 400 V; T_j = 95 ˚C; $I_{T(RMS)}$ = 8 A;dIcom/dt = 3.6 A/ms; gate open circuit	--	20	--	V/µs
Gate controlled turn-on time	t_{gt}	I_{TM} = 12A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5A/µs	--	2	--	µs

Note:

1. Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIACs may switch to the on-state. The rate of rise of current should not exceed 6 A/µs.

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

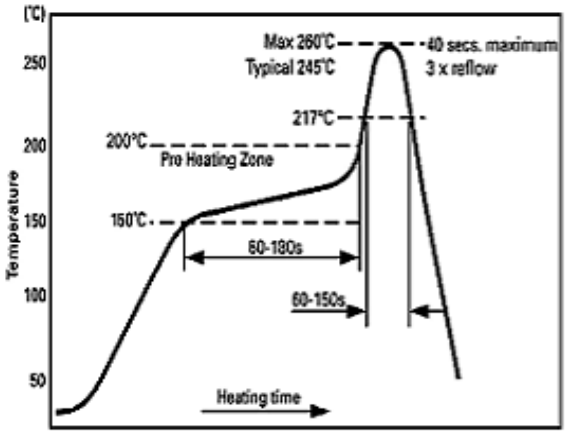
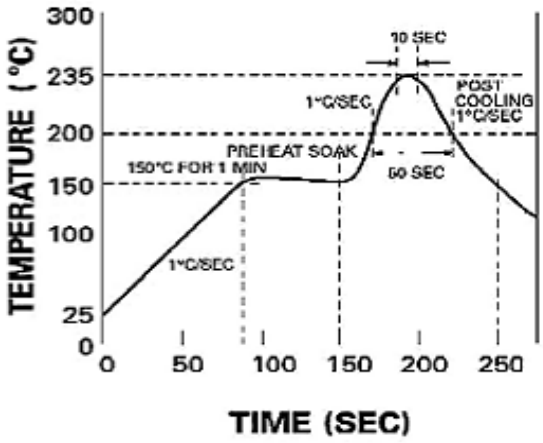


Figure 2

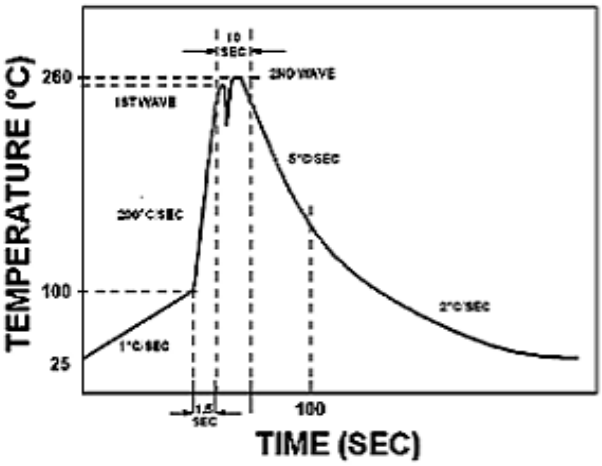


Reflow profiles in tabular form

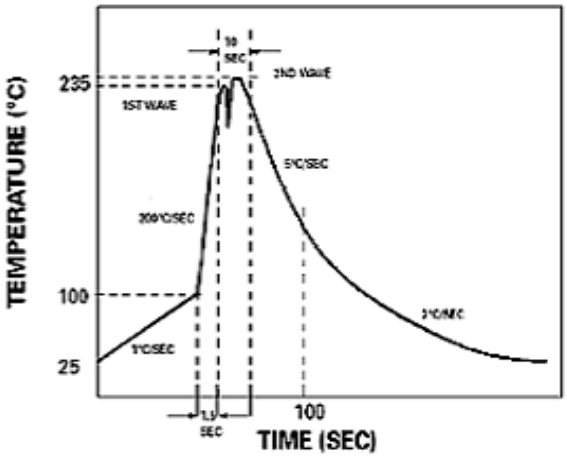
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

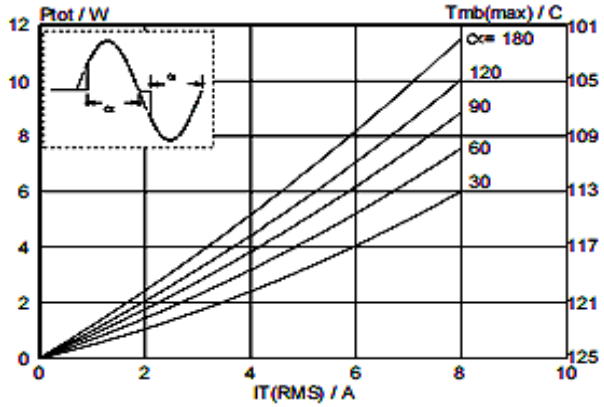


Fig 2: Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, tp ≤ 20ms.

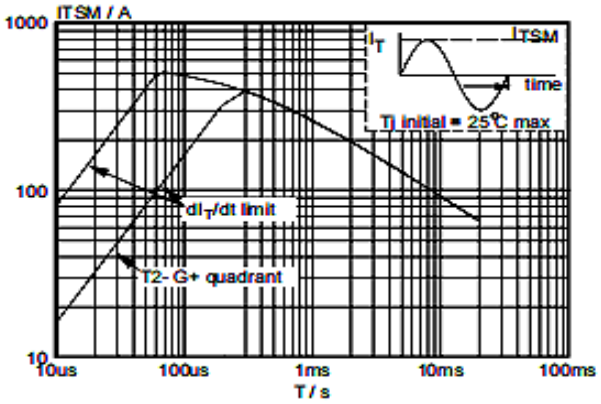


Fig 3: Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

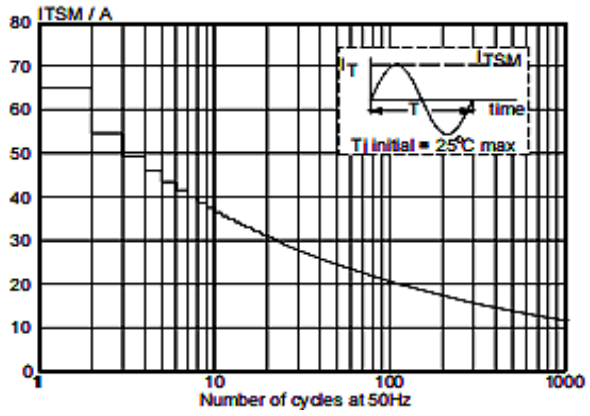


Fig 4: Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

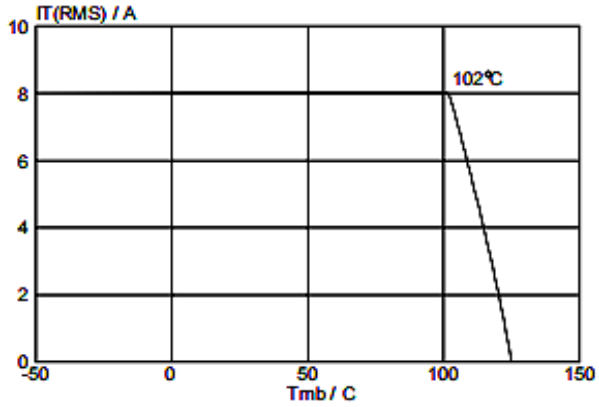


Fig 5: Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents,f = 50Hz;

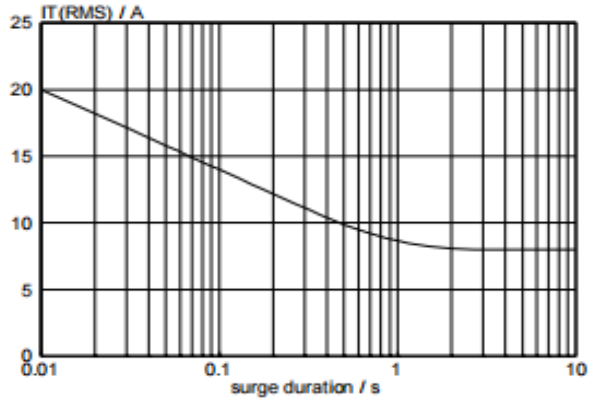
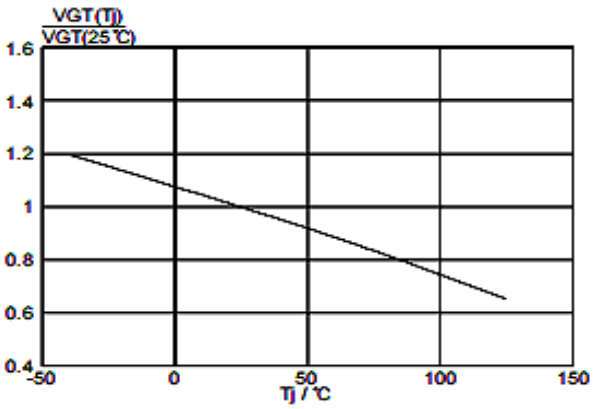


Fig 6: Normalized gate trigger voltage $V_{GT}(Tj)/ V_{GT}(25^{\circ}C)$, versus junction temperature T_j



BT137_600D/800D
Rev03_ 24012023EM

TYPICAL CHARACTERISTICS CURVES

Fig 7: Normalized gate trigger current $I_{GT}(Tj)/I_{GT}(25^{\circ}C)$, versus junction temperature T_j

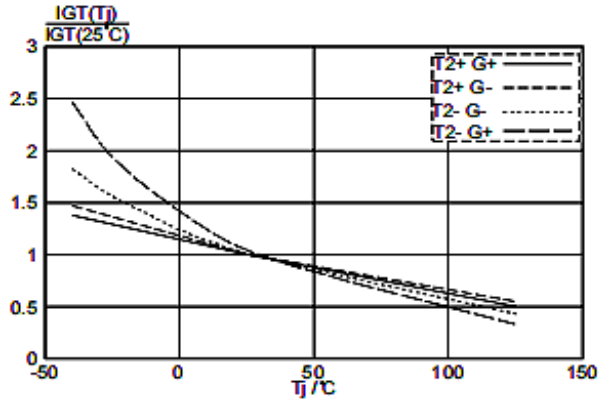


Fig 8: Normalized latching current $I_L(Tj)/I_L(25^{\circ}C)$,versus junction temperature T_j

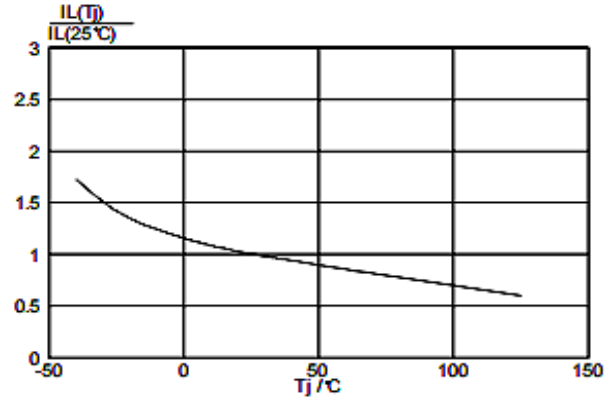


Fig 9: Normalized holding current $I_H(Tj)/I_H(25^{\circ}C)$,versus junction temperature T_j

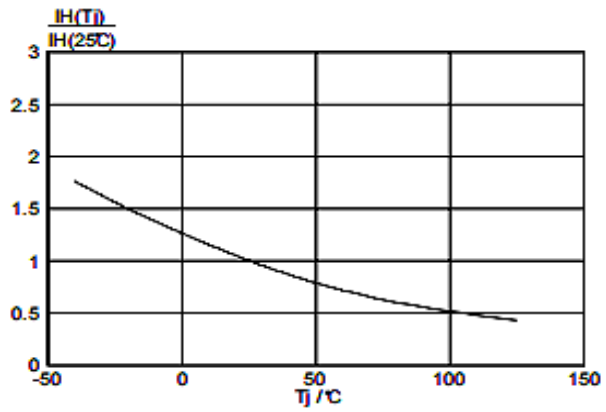


Fig 10: Typical and maximum on-state characteristic.

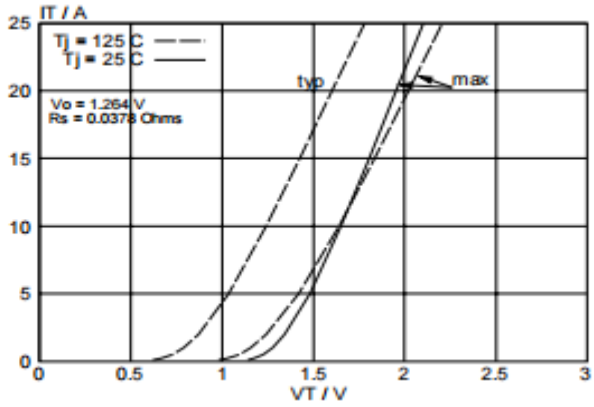


Fig 11: Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus

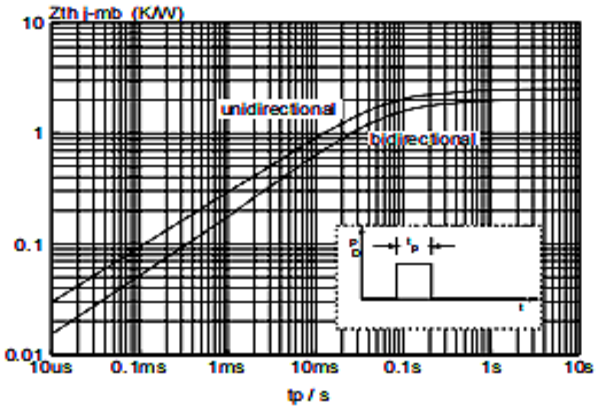
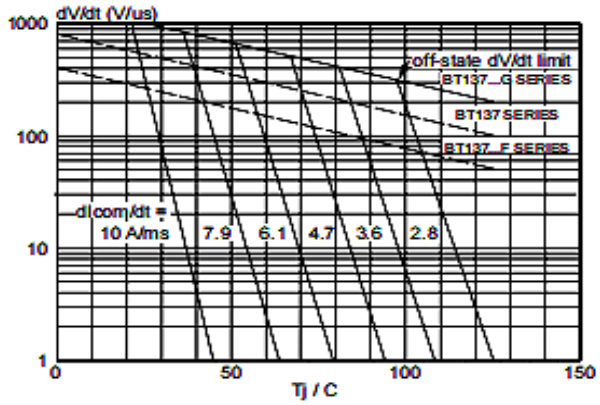
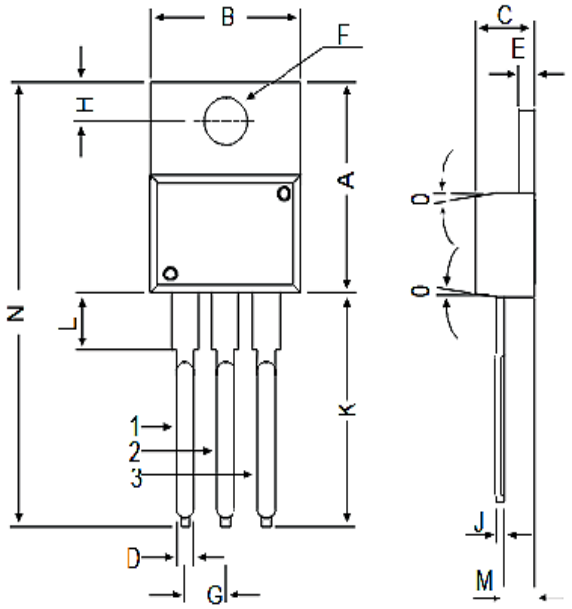


Fig 12: Typical commutation dV/dt versus junction temperature, parameter commutation dI_T/dt. The TRIACs should commutate when the dV/dt is below the value on the appropriate curve for per-commutation



PACKAGE DETAILS

TO-220 Leaded Plastic Package

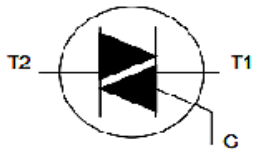


DIM	MIN	MAX
A	14.42	16.51
B	9.63	10.67
C	3.56	4.83
D	—	0.90
E	1.15	1.40
F	3.75	3.88
G	2.29	2.79
H	2.54	3.43
J	—	0.56
K	12.70	14.73
L	2.80	4.07
M	2.03	2.92
N	—	31.24
O	7 DEG	

All Dimensions are in mm

PIN CONFIGURATIONS

1. main terminal 1
2. main terminal 2
3. gate
4. main terminal 2



Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.

CDIL is a registered trademark of
Continental Device India Pvt. Limited
C-120 Naraina Industrial Area, New Delhi 110 028, India.
Telephone +91-11-2579 6150, 4141 1112 Fax +91-11-2579 5290, 4141 1119
email@cdil.com www.cdil.com
CIN No. U32109DL1964PTC004291