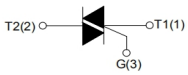
1Amp TRIACs

BT131-600
BT131-800

TO-92



TO-92
Leaded Package
RoHS compliant

DESCRIPTION:

With low holding and latching current, BT131 Series TRIACs are especially recommended for use on middle and small resistance type power load.

MAIN FEATURES:

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	1	A
V_{DRM}/V_{RRM}	600/800	V
V_{TM}	≤1.5	V

APPLICATIONS:

1. General Purpose Bidirectional Switching and Phase Control Applications
2. These Devices are intended to be interfaced directly to Microcontrollers, Logic Integrated Circuits and other Low Power Gate Trigger Circuits

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ℃)

PARAMETER		SYMBOL	VALUE	UNITS
Repetitive Peak Off-State Voltage		V_{DRM}	600/800	V
Repetitive peak reverse voltage		V_{RRM}	600/800	V
RMS On-State Current (Full Sine Wave, T_{lead} < 51°C)		$I_{T(RMS)}$	1.0	A
Non-Repetitive Peak On-State Current (full cycle, F=50Hz)		I_{TSM}	16	A
I^2t value for fusing (t_p=10ms)		I^2t	1.28	A^2s
Critical rate of rise of on-state current (IG=2×IGT)	I-II-III	d_I/dt	50	A/μs
	IV		10	
Peak Gate Current		I_{GM}	2	A
Peak Gate Power		P_{GM}	5	W
Average gate power dissipation		$P_{G(AV)}$	0.5	W
Operating Junction Temperature		T_J	-40~125	°C
Storage Temperature		T_{STG}	-40 ~ 150	°C
THERMAL CHARACTERISTICS				
Thermal Resistance, Junction to Lead		$R_{th(j-c)}$	60	℃/W

BT131-600/800
Rev04_10032024JS

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

PARAMETER	SYMBOL	TEST CONDITION	QUADRANT	VALUE	T	D	UNITS
Gate Trigger Current	I_{GT}	V_D=12V,R_L=33Ω	I-II-III	MAX	3	5	mA
			IV		5	10	
Latching Current	I_L	I_G=1.2I_{GT}	I-III-IV	MAX	5	5	mA
			II		10	20	
Non-triggering gate voltage	V_{GD}	V_D=V_{DRM}	I-II-III-IV	MIN	0.2		V
Gate Trigger Voltage	V_{GT}	V_D=12V,R_L=33Ω	I-II-III-IV	MAX	1.3		V
Holding Current	I_H	I_T=100mA		MAX	5	7	mA
Critical rate of rise of commutating off-state voltage	dV/dt	V_D=0.66×V_{DRM} T_j=125°C Gate open		MIN	20	50	V/µs

STATIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		VALUE		UNITS
Peak on-state voltage drop	V_{TM}	I_{TM}=1.4A t_p=380µs	T_j=25°C	MAX	1.5	V
Gate Controlled Turn-on Time	I_{DRM} I_{RRM}	V_{DRM}= V_{RRM}	T_j=25°C	MAX	5	µA
			T_j=125°C		0.5	mA

Typical Characteristic Curves

FIG.1: Maximum power dissipation vs. RMS on-state current

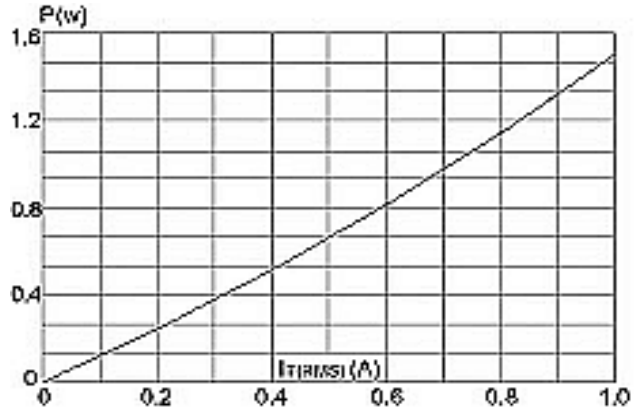


FIG.2: RMS on-state current versus case temperature

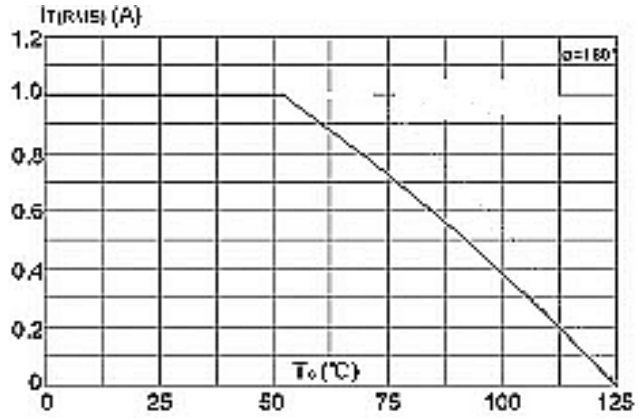


FIG.3: Surge peak on-state current versus number of cycles

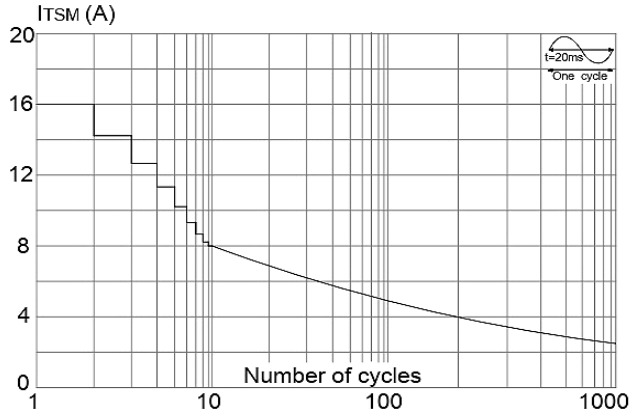


FIG.4:On-state characteristics (maximum values)

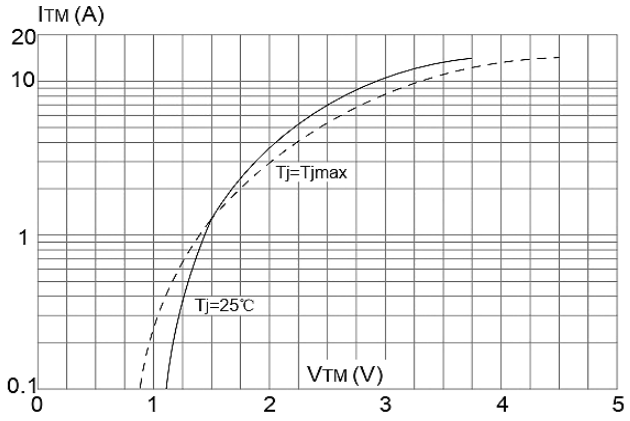


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms, and corresponding value of I2 t (dI/dt < 50A/µs)

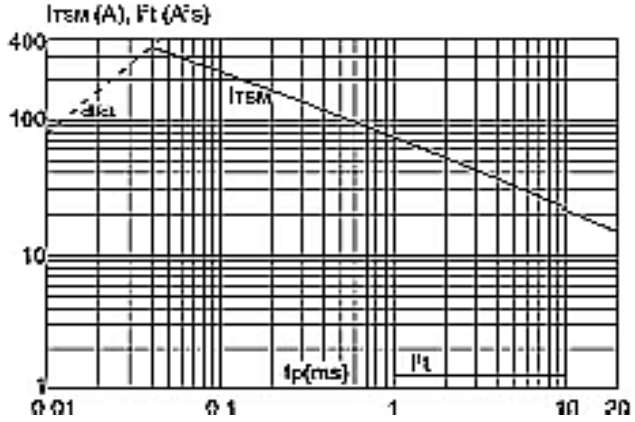
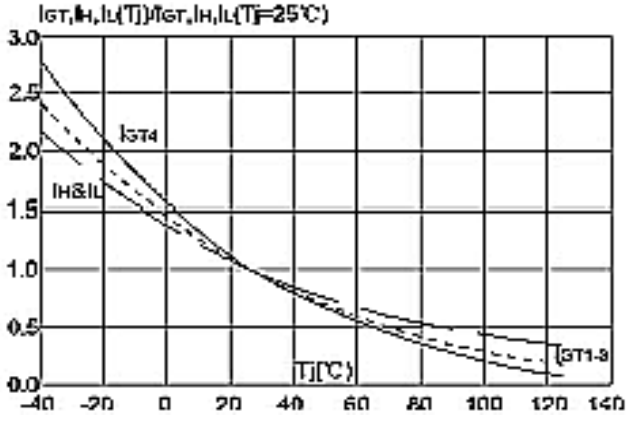


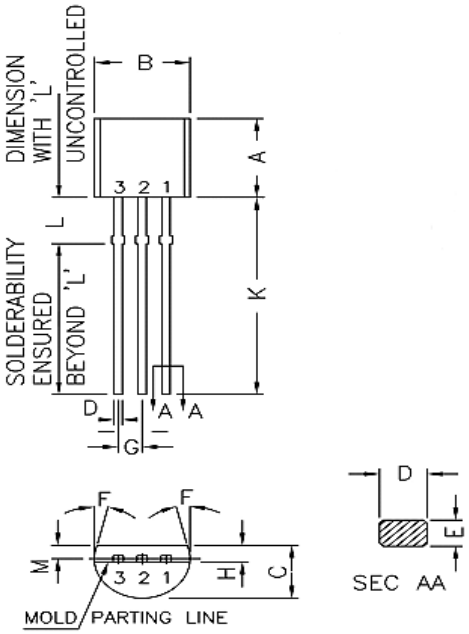
FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



BT131-600/800
Rev04_10032024JS

Package Details

TO-92 Leaded Package

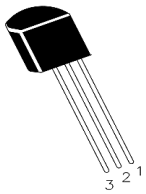


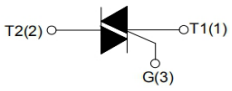
DIM	MIN	MAX
A	4,32	5,33
B	4,45	5,20
C	3,18	4,19
D	0,41	0,55
E	0,35	0,50
F	5 DEG	
G	1,14	1,40
H	1,20	1,40
K	12,70	–
L	1.982	2.082
M	1,03	1,20

ALL DIMENSIONS IN MM

Pin Configuration

1. MT1
2. GATE
3. MT2





Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.
Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

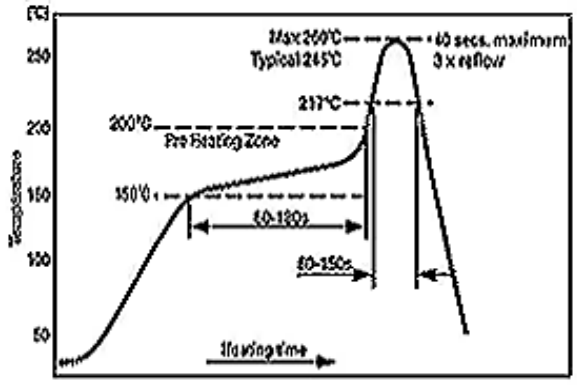
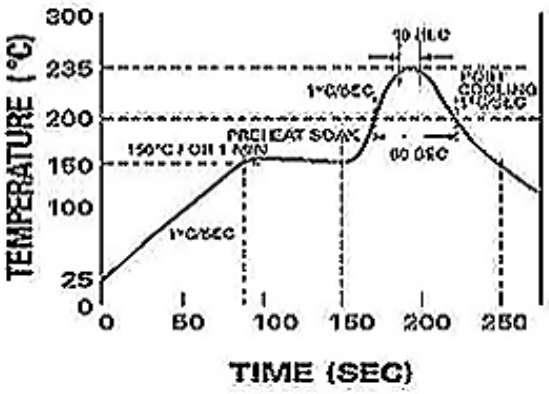


Figure 2

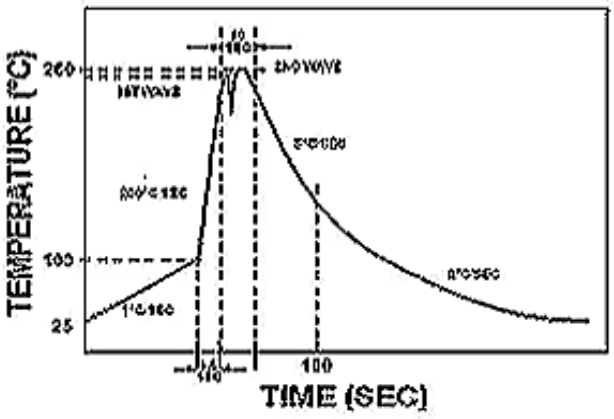


Reflow profiles in tabular form

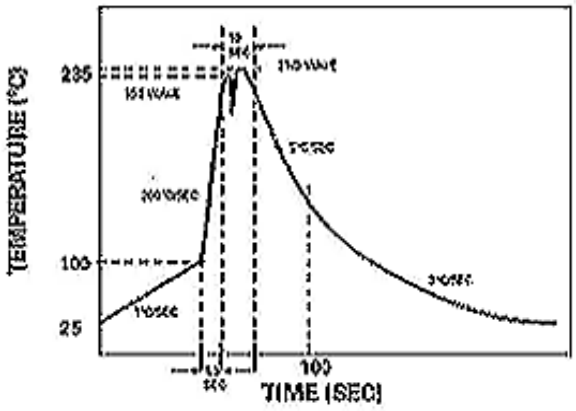
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form		
Profile Feature	**Sn-Pb System**	**Pb-free System**
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max.

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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BT131-600/800
Rev04_10032024JS