TRIACs

BT131-500
BT131-600
BT131-800

TO-92

TO-92
Leaded Package
RoHS compliant

FEATURES: Passivated, Sensitive Gate Triacs

APPLICATIONS:

1. General Purpose Bidirectional Switching and Phase Control Applications
2. These Devices are intended to be interfaced directly to Microcontrollers, Logic Integrated Circuits and other Low Power Gate Trigger Circuits

ABSOLUTE MAXIMUM RATINGS (T_a = 25 ℃)

PARAMETER		SYMBOL	VALUE	UNITS
Repetitive Peak Off-State Voltage	BT131-500	V_{DRM}	500	V
	BT131-600		600	
	BT131-800		800	
RMS On-State Current (Full Sine Wave, T_{lead} < 51°C)		$I_{T(RMS)}$	1	A
Non-Repetitive Peak On-State Current (Full Sine Wave : T_j = 25°C prior to Surge)	t=20ms	I_{TSM}	16	A^2s
	t=16.7ms		17.6	
Circuit Fusing (t=10ms)		I^2t	1.28	
Repetitive Rate of Rise of On-State Current after Triggering (I_{TM}=1.5A, I_G=0.2A, d_{IG}/dt=0.2A/ms)	T2+G+	d_{IT}/dt	50	A/ms
	T2+G-		50	
	T2-G-		50	
	T2-G+		10	
Peak Gate Voltage		V_{GM}	5	V
Peak Gate Current		I_{GM}	2	A
Peak Gate Power		P_{GM}	5	W
Average Gate Power (over any 20ms period)		$P_{G(AV)}$	0.5	W
Operating Junction Temperature		T_J	125	°C
Storage Temperature		T_{STG}	-40 ~ 150	°C

THERMAL CHARACTERISTICS

PARAMETER		SYMBOL	VALUE			UNITS
			MIN	TYP	MAX	
Thermal Resistance, Junction to Lead	Full Cycles	$R_{\theta\ J\text{-}Lead}$	-	-	60	K/W
	Half Cycles		-	-	80	-
Thermal Resistance, Junction to Ambient (PCB Mounted : Lead Length = 4mm)		$R_{\theta\ J\text{-}Amb}$	-	150	-	K/W

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

PARAMETER		SYMBOL	TEST CONDITION	VALUE			UNITS
				MIN	TYP	MAX	
Gate Trigger Current	T2+G+	I_{GT}	V_D=12V, I_T=0.1A	-	0.4	3	mA
	T2+G-			-	1.3	3	
	T2-G-			-	1.4	3	
	T2-G+			-	3.8	7	
Latching Current	T2+G+	I_L	V_D=12V, I_T=0.1A	-	1.2	5	mA
	T2+G-			-	4	8	
	T2-G-			-	1	5	
	T2-G+			-	2.5	8	
On State Voltage		V_T	I_T=2.0A	-	1.2	1.5	V
Gate Trigger Voltage		V_{GT}	V_D=12V, I_T=0.1A	-	0.7	1.5	V
			V_D=400V, I_T=0.1A, T_J=125°C	0.2	0.3	-	
Off State Leakage Current		I_D	V_D=$V_{DRM(MAX)}$, T_J=125°C	-	0.1	0.5	mA
DYNAMIC CHARACTERISTICS							
Holding Current		I_H	V_D=12V, I_{GT}=0.1A	-	1.3	5	mA
Critical rate of Rise of Off State Voltage		dV_D/dt	V_{DM} = 67% $V_{DRM(MAX)}$, T_J=125°C, Exponential Waveform, R_{GK}=1KW	5	15	-	V/µs
Gate Controlled Turn-on Time		t_{gt}	I_{TM}=1.5A, V_D=$V_{DRM(MAX)}$, I_G=0.1A, dI_G/dt= 5A/ms	-	2	-	µs

Typical Characteristic Curves

Fig 1: Maximum on-state Dissipation plot vs RMS on-state current, $I_{T(RMS)}$, Wheres = conduction angle.

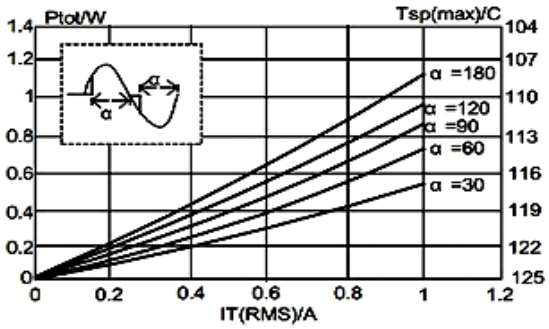


Fig 2: Maximum Permissible Repetitive RMS On-state Current $I_{T(RMS)}$ vs Surge During, For Sinusoidal Current f=50Hz, Tlead≤51°C

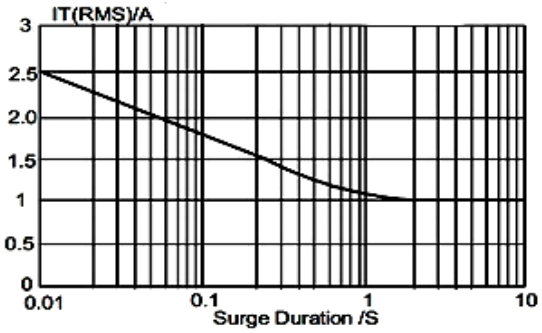


Fig 3: Normalized Gate Trigger Current $I_{GT}(T_J)/I_{GT}(25°C)$ vs Junction Temperature T_j

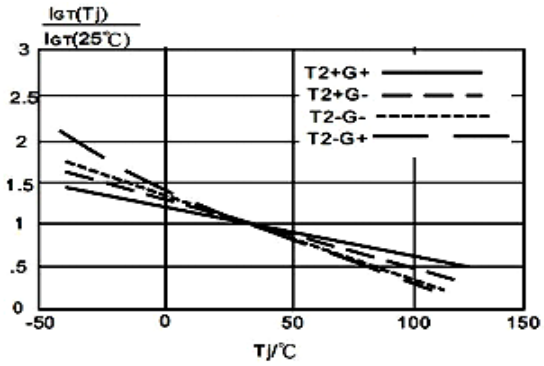


Fig 4: Maximum Permissible Non-Repetitive Peak On-state Current I_{TMS} vs plus width tp for sinusoidal current tp≤20ms

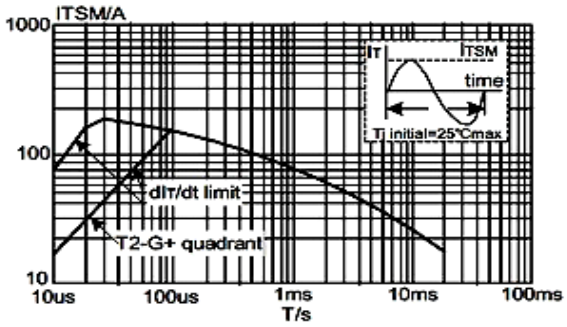


Fig 5: Normalized Gate trigger voltage $V_{GT}(T_J)/V_{GT}(25°C)$ vs Junction Temperature T_J

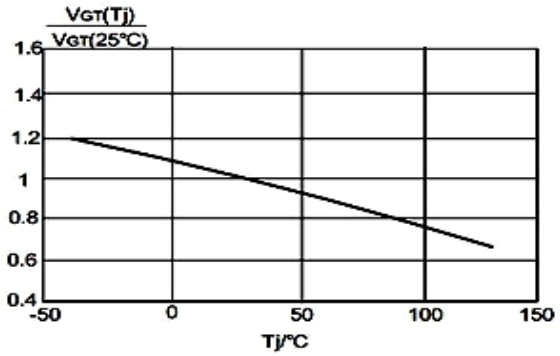
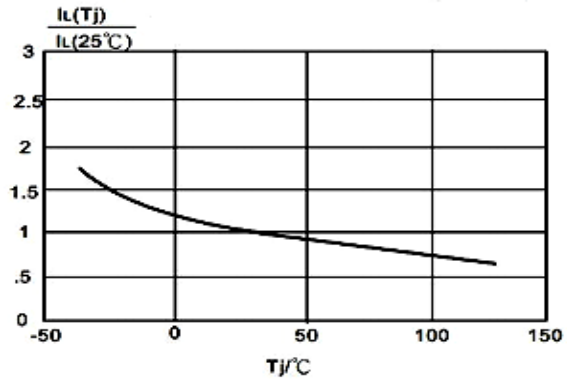


Fig 6: Normalized Latching current $I_L(T_J)/I_L25°C$ vs Junction Temperature T_j



Typical Characteristic Curves

Fig 7: Normalized Holding current
$I_H(T_J)/I_H(25°C)$ vs Junction Temperature

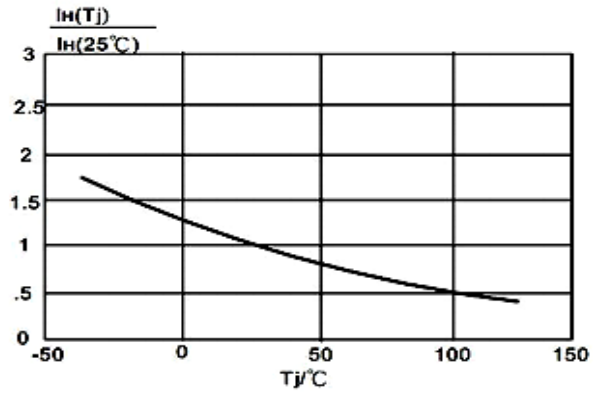


Fig 8: Transient Thermal Impedance Z^{th}
J-lead vs pulse Width tp

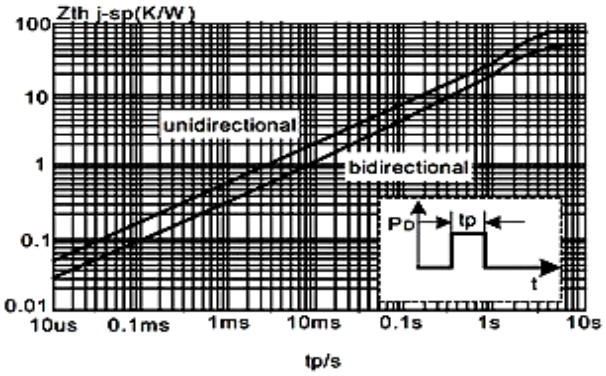


Fig 9: Typical and Maximum On-state Characteristics

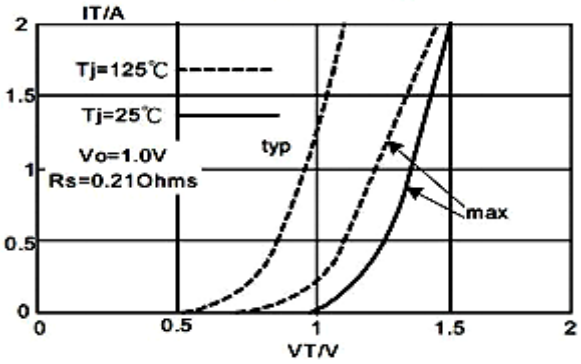
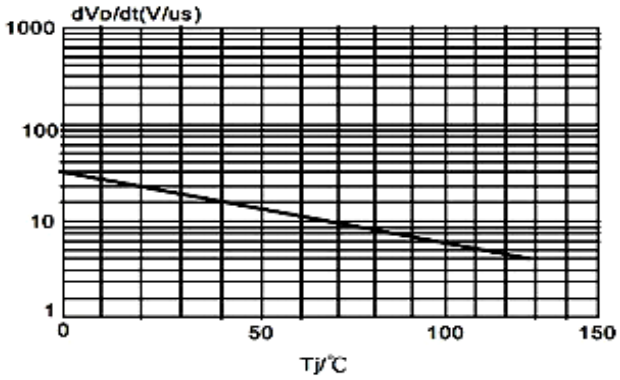
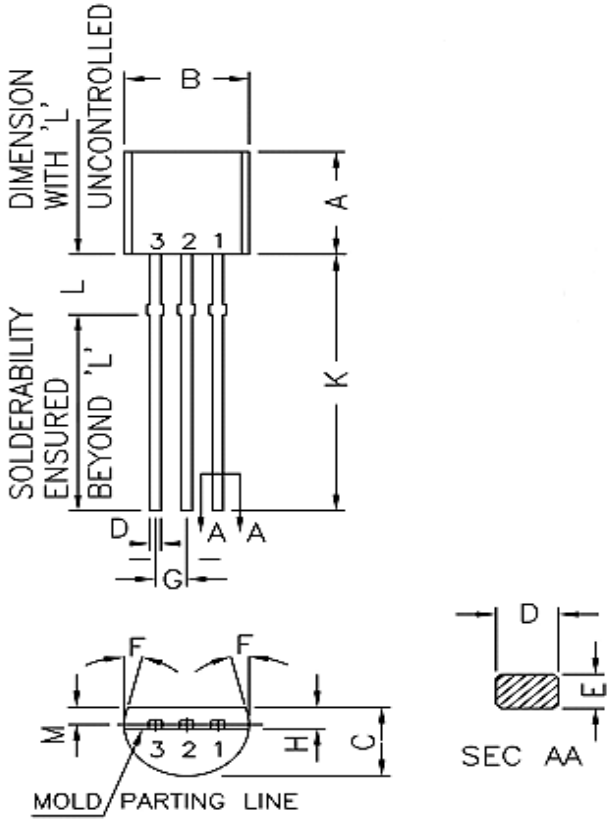


Fig 10: Typical Critical Rate of rise of off-state Voltage dV_D/dt vs Junction Temperature Tj



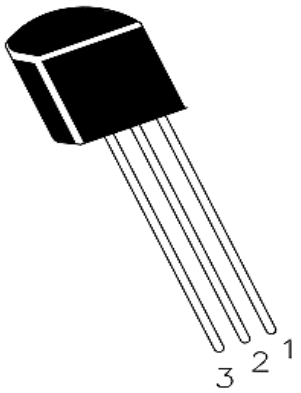
Package Details

TO-92 Leaded Package



DIM	MIN	MAX
A	4,32	5,33
B	4,45	5,20
C	3,18	4,19
D	0,41	0,55
E	0,35	0,50
F	5 DEG	
G	1,14	1,40
H	1,20	1,40
K	12,70	–
L	1.982	2.082
M	1,03	1,20

ALL DIMENSIONS IN MM



Pin Configuration

1. MT2
2. GATE
3. MT1

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).
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