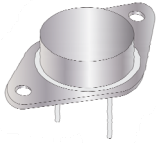


## DARLIGTON COMPLIMENTARY POWER TRANSISTORS



TO-3

**2N6059 NPN**  
**2N6058 NPN**  
**2N6052 PNP**  
**2N6051 PNP**

**TO-3**  
**Metal Can Package**  
**RoHS compliant**

### FEATURE:

1. High DC Current Gain  $H_{fe} = 3500$  (Typ.) @  $I_C = 5.00A$  DC  
 Collector–Emitter Sustaining Voltage @ 100 mA  
 $V_{CEO(SUS)} = 80 V_{DC}$  (Min.)--- 2N6058  
 $= 100 VDC$  (Min.)--- 2N6059, 2N6052
2. Monolithic Construction with Built–In Base–Emitter Shunt Resistors
3. This product is available in AEC-Q101 Compliant and PPAP Capable also.

**Note:** For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

**APPLICATION:** General–purpose amplifier and low frequency switching. switching applications.

### ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	2N6051 2N6058	2N6052 2N6059	UNIT
Collector-Emitter Voltage	$V_{CEO}$	80	100	V
Collector-Base Voltage	$V_{CB}$	80	100	V
Emitter-Base Voltage	$V_{EB}$	5.0		V
Collector Current - Continuous	$I_C$	12		A
Collector Current - Peak		20		A
Base Current	$I_B$	0.2		A
Total Device Dissipation @ $T_C = 25^\circ C$	$P_D$	150		W
Dearate above 25°C		0.857		W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200		°C

### THERMAL RESISTANCE

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
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**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	VALUE		UNIT	
			MIN	MAX		
<b>Off Characteristics</b>						
Collector-Emitter Sustaining Voltage <sup>1</sup>	2N6051 2N6058	$V_{CEO(sus)}$	$I_C = 100\text{mA}, I_B = 0$	80	--	V
	2N6052 2N6059			100	--	
Collector Cutoff Current	2N6051 2N6058	$I_{CEO}$	$V_{CE} = 40\text{V}, I_B = 0$	--	1.0	mA
	2N6052 2N6059			$V_{CE} = 50\text{V}, I_B = 0$	--	
Collector Cutoff Current		$I_{CEX}$	$V_{CE} = \text{Rated } V_{CEO}, V_{BE(off)} = 1.5\text{V}$	--	0.5	mA
			$V_{CE} = \text{Rated } V_{CEO}, V_{BE(off)} = 1.5\text{V}$ $T_C = 150^\circ\text{C}$	--	5.0	mA
Emitter Cutoff Current		$I_{EBO}$	$V_{BE} = 5.0\text{V}, I_C = 0$	--	2.0	mA

**On Characteristics**

DC Current Gain	$h_{FE}$		$I_C = 6.0\text{A}, V_{CE} = 3.0\text{V}$	750	18.000	
			$I_C = 12\text{A}, V_{CE} = 3.0\text{V}$	100	--	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$		$I_C = 6.0\text{A}, I_B = 24\text{mA}$	--	2.0	V
			$I_C = 12\text{A}, I_B = 120\text{mA}$	--	3.0	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$		$I_C = 12\text{A}, I_B = 120\text{mA}$	--	4	V
Base-EMitter On Voltage	$V_{BE(on)}$		$I_C = 6.0\text{A}, V_{CE} = 3.0\text{V}$	--	2.8	V

**Dynamic Characteristics**

Magnitude of common Emitter Small - Signal Short Circuit Forward Current Transfer Ratio	$ h_{fe} $		$I_C = 5.0\text{A}, V_{CE} = 3.0\text{V}, f = 1.0\text{MHz}$	4.0	--	MHz
Output Capacitance	$C_{ob}$		$V_{CE} = 10\text{V}, I_E = 0, f = 1.0\text{MHz}$	--	500	pF
				--	300	
Small-Signal Current Gain	$h_{fe}$		$I_C = 5.0\text{A}, V_{CE} = 3.0\text{V}, f = 1.0\text{MHz}$	300	--	

Note:

1. Pulse test: Pulse Width = 300 $\mu\text{s}$ , Duty Cycle  $\leq 2\%$

### Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

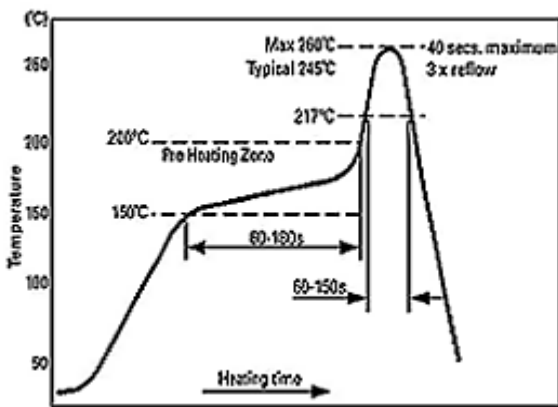
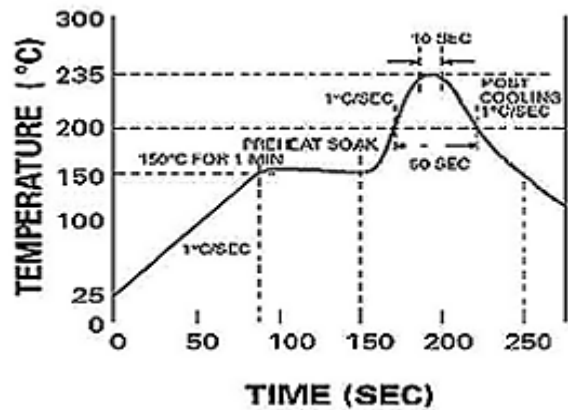


Figure 1

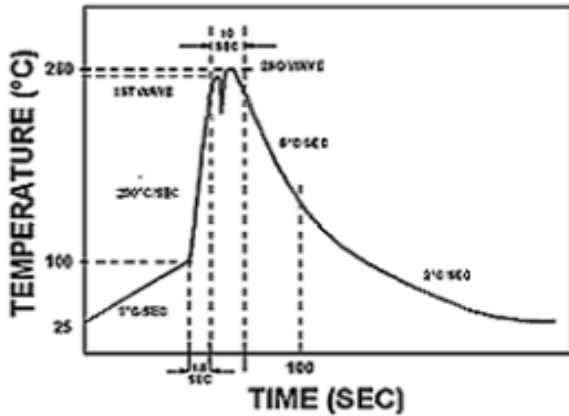


#### Reflow profiles in tabular form

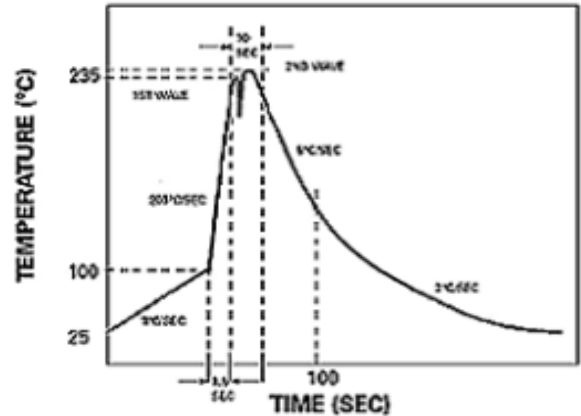
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
<b>Preheat</b>		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Time	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

### Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder

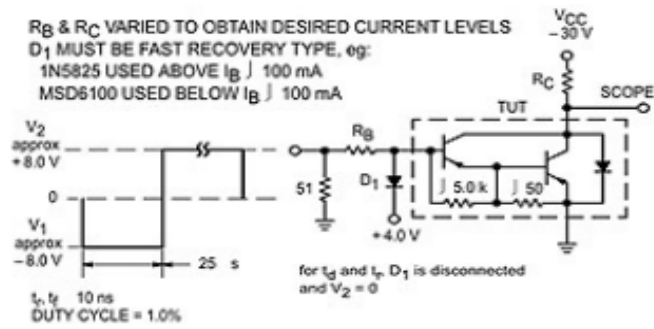


### Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

## TEST CIRCUIT AND DIAGRAMS

### Switching Time Test Circuit



For NPN test circuit reverse diode and voltage polarities.

## TYPICAL CHARACTERISTICS CURVES

Fig 1: Power Derating

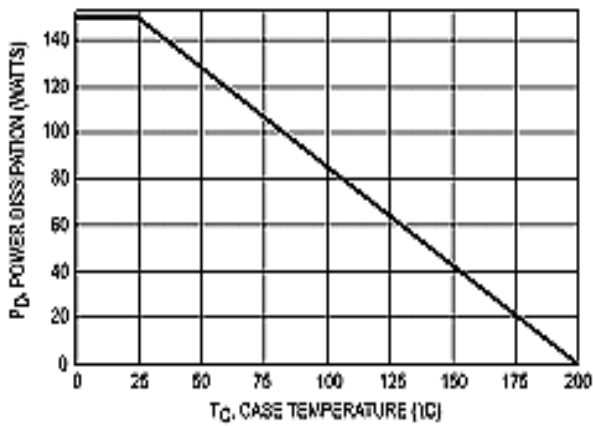


Fig 2: Switching Time

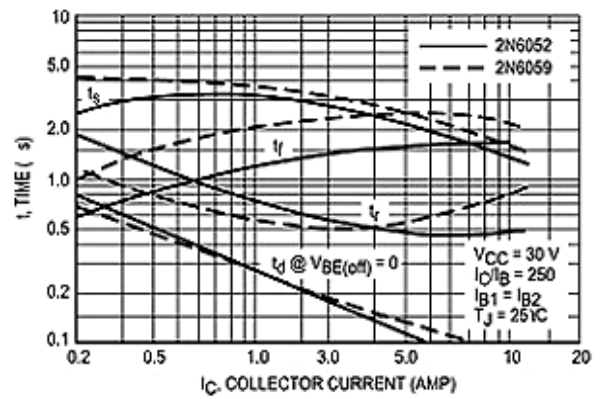
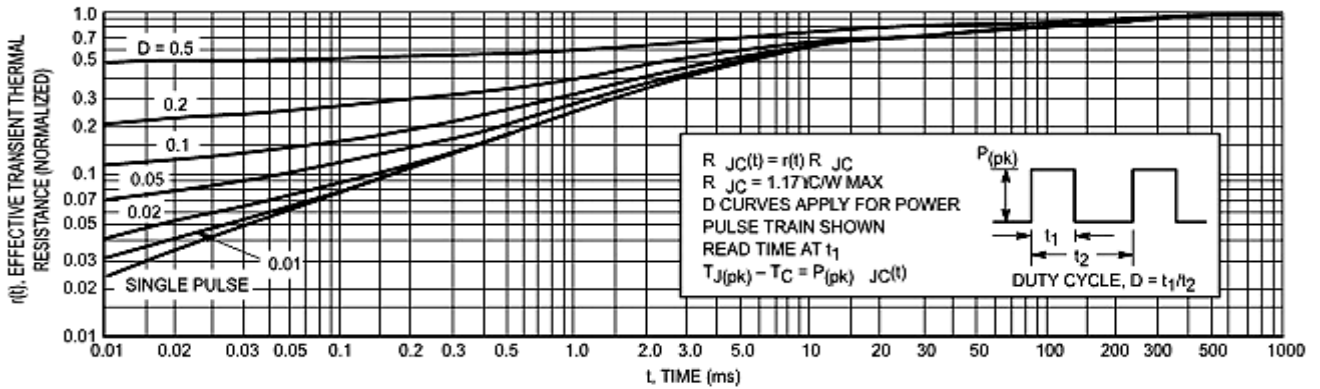


Figure 3. Switching Times

Fig 3: Thermal Response



## TYPICAL CHARACTERISTICS CURVES

Fig 4: 2N6058,2N6051

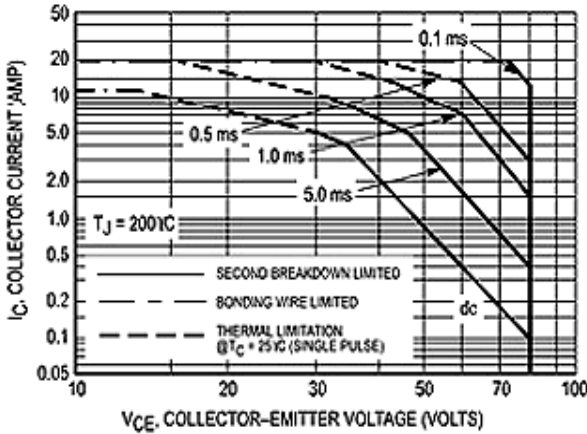


Fig 5: Small Signal Current Gain

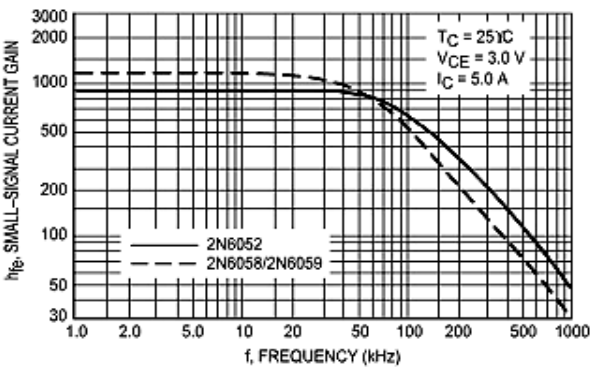


Fig 6: 2N6059,2N6052

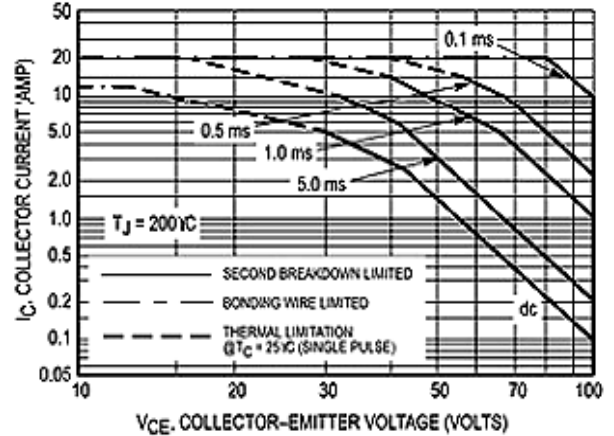


Fig 7: Capacitance

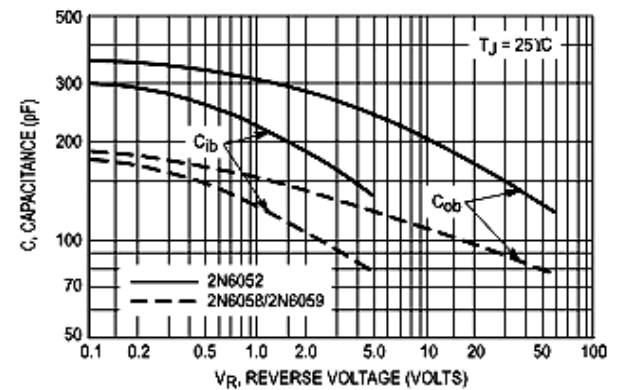
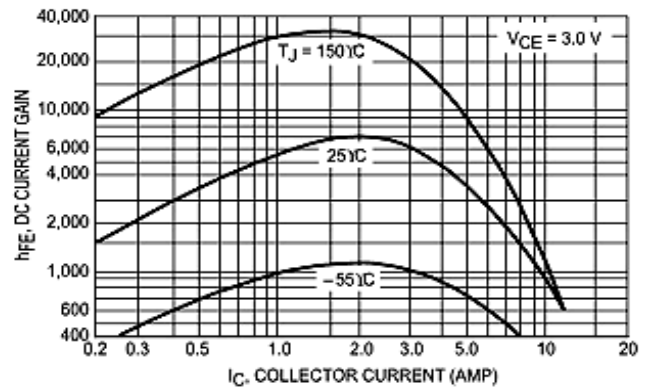
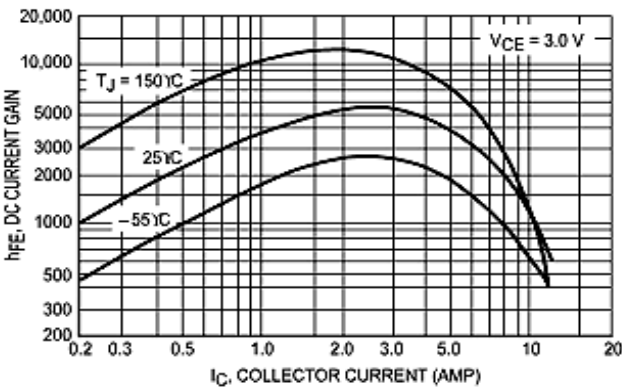


Fig 8: DC Current Gain



## TYPICAL CHARACTERISTICS CURVES

Fig 9: Collector Saturation Region

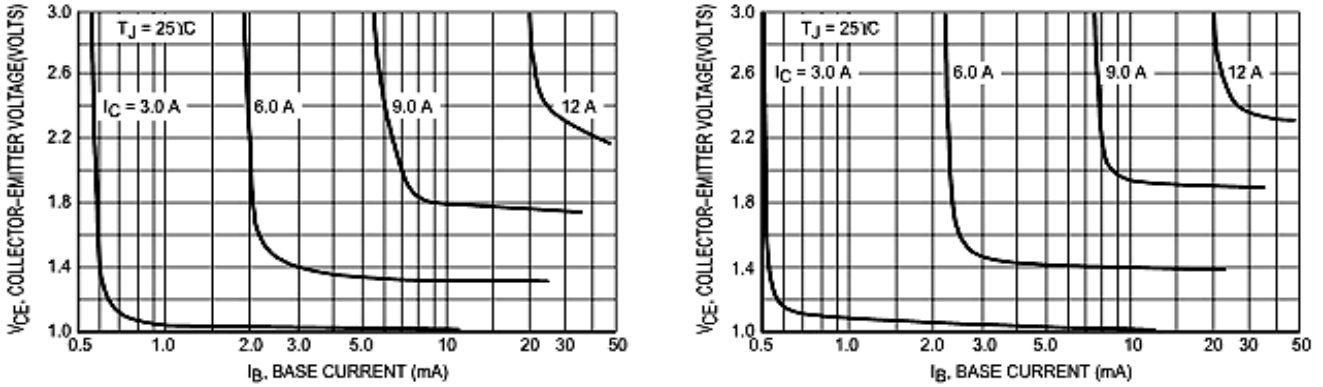
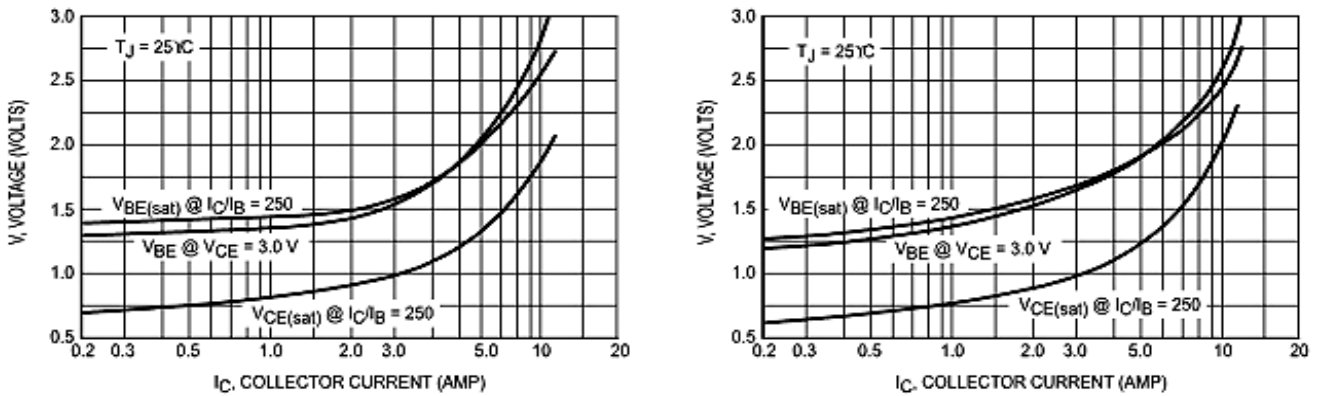


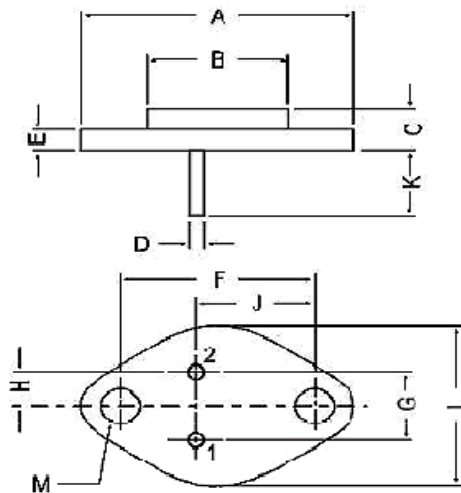
Fig 10: "On" Voltage





## PACKAGE DETAILS

### TO-3 Metal Can Package

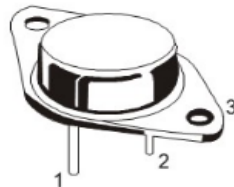


DIM	MIN	MAX
A	--	39.37
B	--	22.22
C	6.35	8.50
D	0.96	1.09
E	--	1.77
F	29.90	30.40
G	10.69	11.18
H	5.20	5.72
J	16.64	17.15
K	11.15	12.25
L	--	26.67
M	3.84	4.19

All Dimension are in mm

### PIN CONFIGURATION

1. BASE
2. EMITTER
3. COLLECTOR



### Packing Detail

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-3	100 pcs/pkt	1.3 kg/100 pcs	12.5" x 8" x 1.8"	0.1K	17" x 11.5" x 21"	2K	27.5 kgs



Continental Device India Pvt. Limited

An IATF 16949, ISO9001 and ISO 14001 Certified Company



## Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

### Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

### Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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## Customer Notes

### Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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