NPN Epitaxial Planar Silicon High Voltage Transistor 2N5551

TO-92

TO-92
Plastic Package
RoHS compliant

FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

Note: For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

APPLICATION:

1. High Voltage NPN Transistor For General Purpose And Telephony Applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Collector -Emitter Voltage	V_{CEO}	160	V
Collector -Base Voltage	V_{CBO}	180	V
Emitter -Base Voltage	V_{EBO}	6.0	V
Collector Current Continuous	I_C	600	mA
Power Dissipation @Ta=25°C	P_D	625	mW
Derate Above 25°C		5.0	mW/°C
Power Dissipation @Tc=25°C	P_D	1.5	W
Derate Above 25°C		12	mW/°C
Operating And Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150	°C
Junction to Case	$R_{th(j-c)}$	125	°C/W
Junction to Ambient	$R_{th(j-a)}$ [1]	357	

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector -Emitter Voltage	V_{CEO}	I_C=1mA,I_B=0	160	--	--	V
Collector -Base Voltage	V_{CBO}	I_C=100uA.I_E=0	180	--	--	V
Emitter -Base Voltage	V_{EBO}	I_E=10uA, I_C=-0	6.0	--	--	V
Collector-Cut off Current	I_{CBO}	V_{CB}=160V, I_E=0	--	--	50	nA
		V_{CB}=160V, I_E=0, T_a=100°C	--	--	50	µA
Emitter-Cut off Current	I_{EBO}	V_{EB}=4V, I_C=0	--	--	50	nA
DC Current Gain	h_{FE}	I_C=1mA,V_{CE}=5V	80	--	--	
		I_C=10mA,V_{CE}=5V	80	--	250	
		I_C=50mA,V_{CE}=5V	30	--	--	

ELECTRICAL CHARACTERISTICS at (Ta = 25 ℃ Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector Emitter Saturation Voltage	$V_{CE(Sat)}$ [1]	I_C=10mA,I_B=1mA	--	--	0.15	V
		I_C=50mA,I_B=5mA	--	--	0.2	V
Base Emitter Saturation Voltage	$V_{BE(Sat)}$ [1]	I_C=10mA,I_B=1mA	--	--	1.0	V
		I_C=50mA,I_B=5mA	--	--	1.0	V

Dynamic Characteristics

Small Signal Current Gain	hfe	I_C=1mA, V_{CE}=10V, f=1KHz	50	--	200	
Transition Frequency	ft	V_{CE}=10V,I_C=10mA, f=100MHz	100	--	300	MHz
Output Capacitance	Cob	V_{CB}=10V, I_E=0, f=1MHz	--	--	6.0	pF
Input Capacitance	Cib	V_{EB}=0.5V, I_C=0, f=1MHz	--	--	20	pF
Noise Figure	NF	V_{CE}=5V, I_C=250uA, R=1kohm, f=10Hz to 15.7kHz	--	--	8.0	dB

Note:

1. Pulse Test: Pulse Width=300us, Duty Cycle=2%

Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

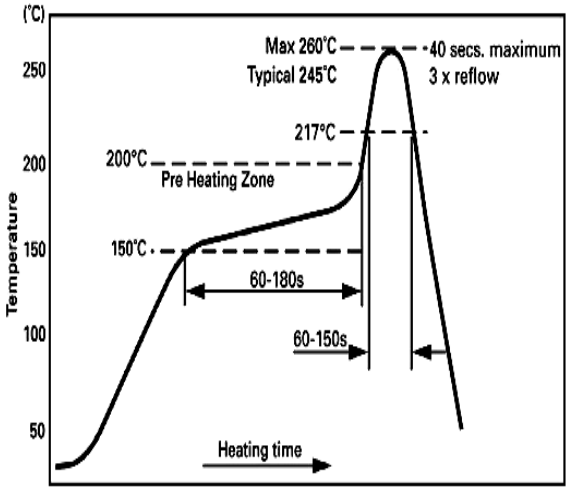
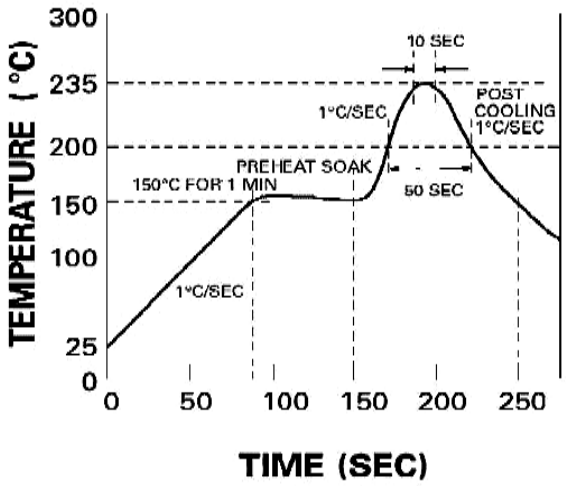


Figure 2

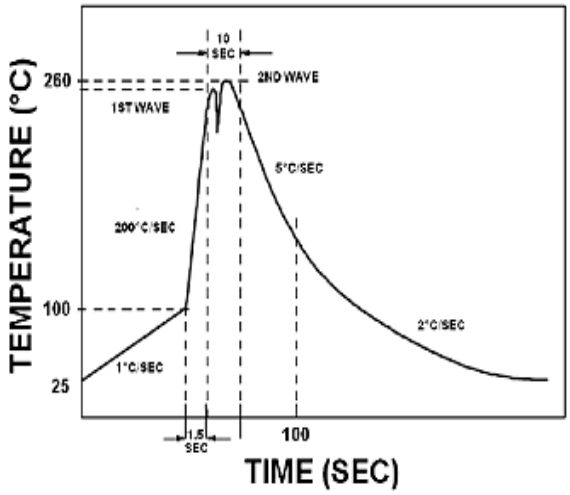


Reflow profiles in tabular form

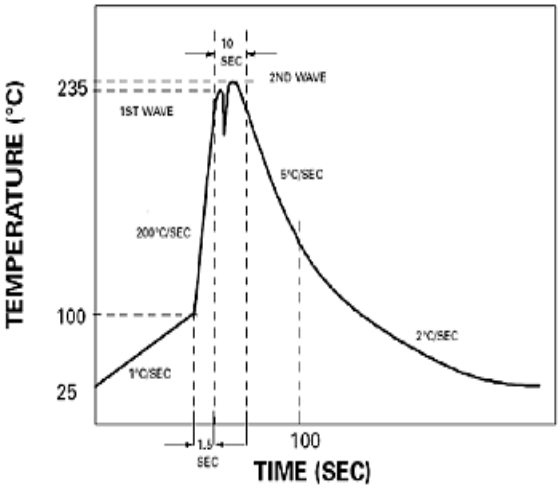
Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
Preheat – Temperature Range – Time	 150-170°C 60-180 seconds	 150-200°C 60-180 seconds
Time maintained above: – Temperature – Time	 200°C 30-50 seconds	 217°C 60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used



The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max

TYPICAL CHARACTERISTICS CURVES

Fig 1: Typical Pulsed Current Gain vs Collector Current

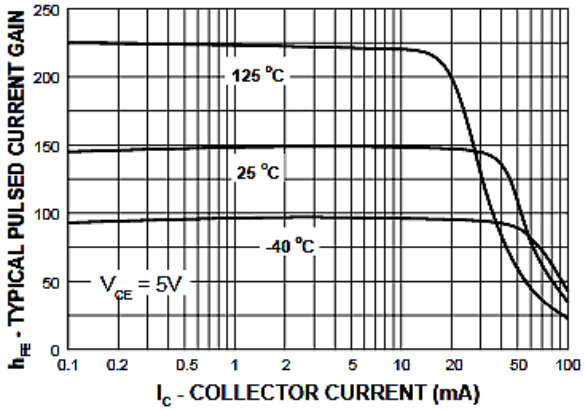


Fig 2: Base-Emitter Saturation Voltage vs Collector Current

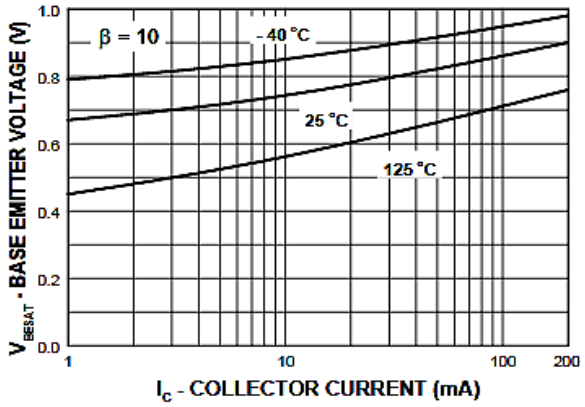


Fig 3: Collector Cutoff Current vs Ambient Temperature

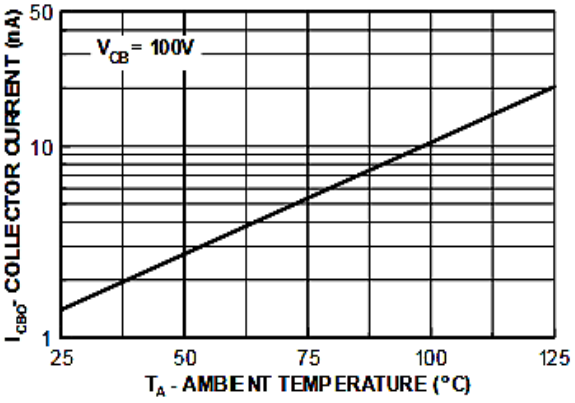


Fig 4: Collector-Emitter Saturation Voltage vs Collector Current

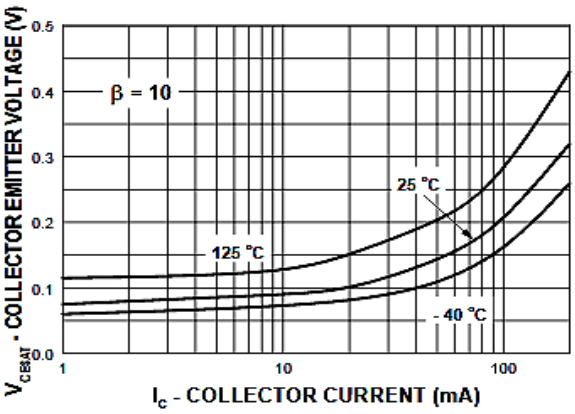


Fig 5: Base-Emitter On Voltage vs Collector Current

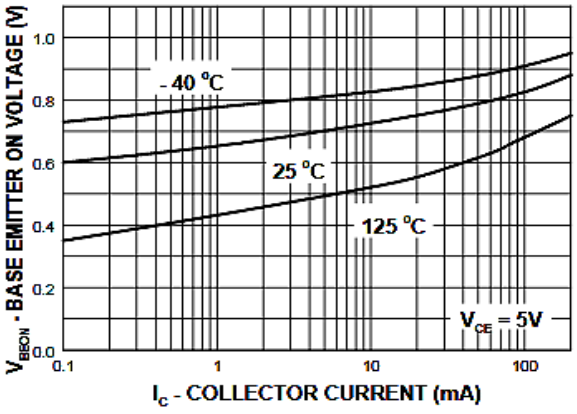
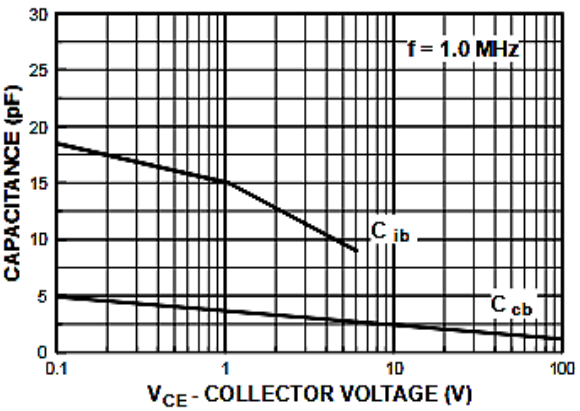


Fig 6: Input and Output Capacitance vs Reverse Voltage



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TYPICAL CHARACTERISTICS CURVES

Fig 7: Collector- Emitter Breakdown Voltage with Resistance Between Emitter-Base

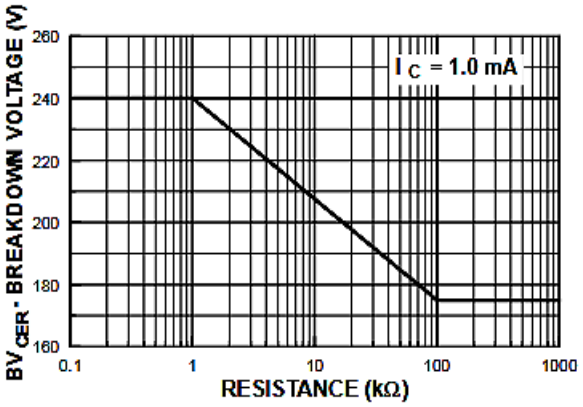


Fig 8: Power Dissipation vs Ambient Temperature

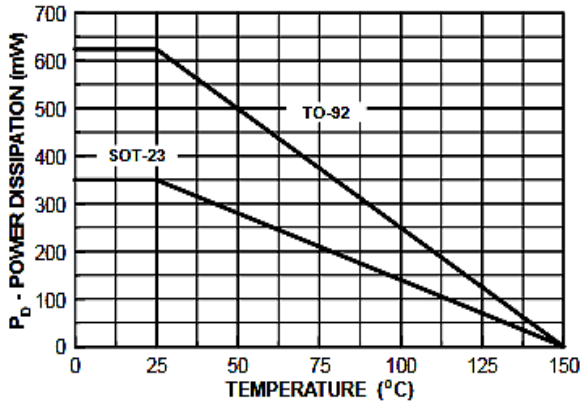
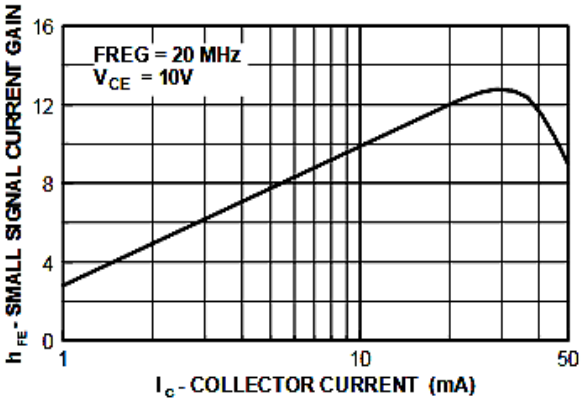
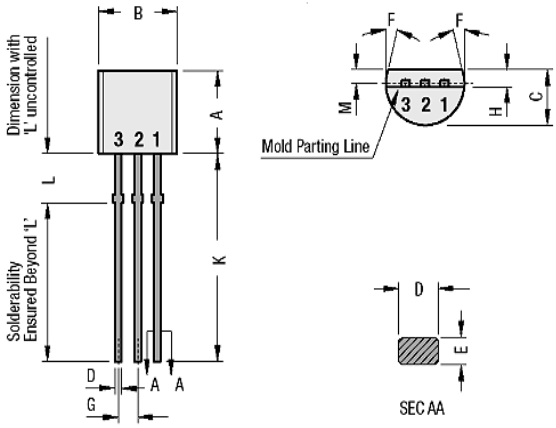


Fig 9: Small Signal Current Gain vs Collector Current



PACKAGE DETAILS

TO-92 Leaded Plastic Package

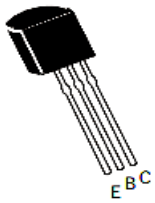


DIM	MIN	MAX
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	
G	1.14	1.40
H	1.20	1.40
K	12.7	
L	1.982	2.082
M	1.03	1.20

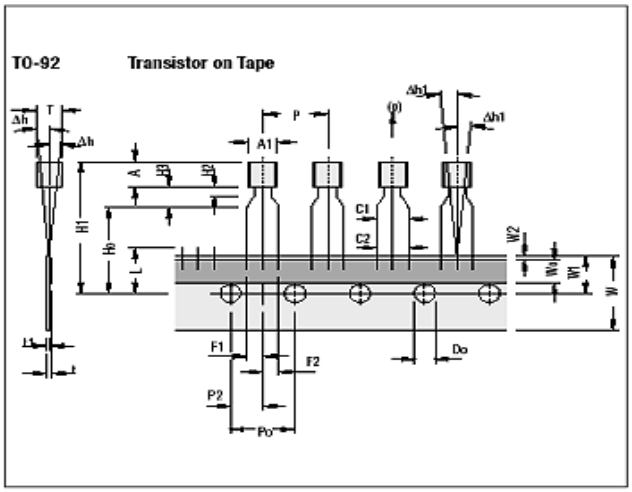
All Dimensions are in mm

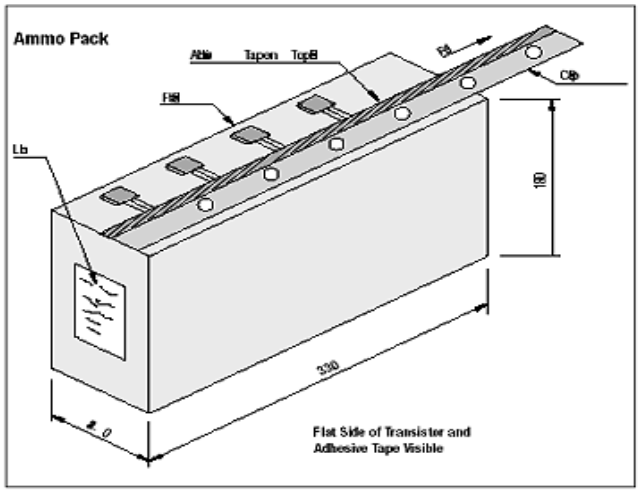
PIN CONFIGURATION

1. Collector
2. Base
3. Emitter



TO-92 Tape and Ammo Packaging





All Dimensions are in mm

Tape Specifications

Item description	Symbol	TO-92 Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component[Cr]	P		12.7		±1.0
Feed hole pitch[§1]	Po		12.7		±0.3
Feed hole center to component centre[§2]	P2		6.35		±0.4
Comp. alignment, Side view[§3]	Dh		0	1.0	
Comp. alignment, Front view[§3]	Dh1		0	1.3	
Tape width[Cr]	W		18		±0.5
Hold down tape width[Cr]	Wo		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of snipped leads	L			11.0	
Feed hole diameter[Cr]	Do		4		±0.2
Total tape thickness[§4]	t			1.2	
Lead-to-lead distance[Cr]	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelismCr	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.
§2 To be measured at bottom of clinch.
§3 At top of body.
§4 t1 = 0.3 – 0.6 mm
Cr Critical Dimension.

All Dimensions are in mm

Packaging Information

Package/Case Type	Packaging Type	Std. Packing	Inner Carton			Outer Carton		
		Qty	Qty	Size L x W x H (cm)	Gross Weight (Kg)	Qty	Size L x W x H (cm)	Gross Weight (Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

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Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.
If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.
The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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