



Continental Device India Pvt. Limited

An IATF 16949, ISO9001 and ISO 14001/ISO 45001 Certified Company



## PNP SILICON PLANAR EPITAXIAL SWITCHING TRANSISTORS



TO-92

**2N3905**  
**2N3906**

**TO-92**  
**Plastic Package**  
**RoHS compliant**

### FEATURE:

1. This product is available in AEC-Q101 Compliant and PPAP Capable also.

**Note:** For AEC-Q101 compliant products, please use suffix -AQ in the part number while ordering.

**APPLICATIONS:** General Purpose Switching And Amplifier Applications

### ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT
Collector Emitter Voltage	$V_{CEO}$	40	V
Collector Base Voltage	$V_{CBO}$	40	V
Emitter Base Voltage	$V_{EBO}$	5.0	V
Collector Current Continuous	$I_C$	200	mA
Power Dissipation Ta=25°C	$P_D$	625	mW
Derate Above 25°C		5.0	mW/°C
Power Dissipation Ta=60°C	$P_D$	250	mW
Power Dissipation Tc=25°C	$P_D$	1.5	W
Derate Above 25°C		12	mW/°C
Operating And Storage Junction Temperature Range	$T_j, T_{stg}$	-55 to +150	°C

### THERMAL RESISTANCE

Junction to Case	$R_{th(j-c)}$	83.3	°C/W
Junction to Ambient in free air	$R_{th(j-a)}$	200	

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**ELECTRICAL CHARACTERISTICS at** (Ta = 25 °C Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	Min/Max	2N3905	2N3906	UNIT
Collector Emitter Voltage	$V_{CEO}$	$I_C=1mA, I_B=0$	Min	40	40	V
Collector Base Voltage	$V_{CBO}$	$I_C=10mA, I_E=0$	Min	40	40	V
Emitter Base Voltage	$V_{EBO}$	$I_E=10mA, I_C=0$	Min	5.0	5.0	V
Collector Cut Off Current	$I_{CEX}$	$V_{CE}=30V, V_{EB}=3V$	Max	50	50	nA
Base Cut Off Current	$I_{BL}$	$V_{CE}=30V, V_{EB}=3V$	Max	50	50	nA
DC Current Gain	$hFE^1$	$I_C=0.1mA, V_{CE}=1V$	Min	30	60	
		$I_C=1mA, V_{CE}=1V$	Min	40	80	
		$I_C=10mA, V_{CE}=1V$		50 ~ 150	100~300	
		$I_C=50mA, V_{CE}=1V$	Min	30	60	
		$I_C=100mA, V_{CE}=1V$	Min	15	30	
Collector Emitter Saturation Voltage	$V_{CE(sat)}^1$	$I_C=10mA, I_B=1mA$	Max	0.25	0.25	V
		$I_C=50mA, I_B=5mA$	Max	0.40	0.40	V
Base Emitter Saturation Voltage	$V_{BE(sat)}^1$	$I_C=10mA, I_B=1mA$		0.65~0.85	0.65~0.85	V
		$I_C=50mA, I_B=5mA$	Max	0.95	0.95	V

**Note:**

1. Pulse Condition: =300 $\mu$ s, Duty Cycle=2%
2. For PNP device voltage and current values will be negative (-).

### Recommended Reflow Solder Profiles

The recommended reflow solder profiles for Pb and Pb-free devices are shown below.

Figure 1 shows the recommended solder profile for devices that have Pb-free terminal plating, and where a Pb-free solder is used.

Figure 2 shows the recommended solder profile for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 1

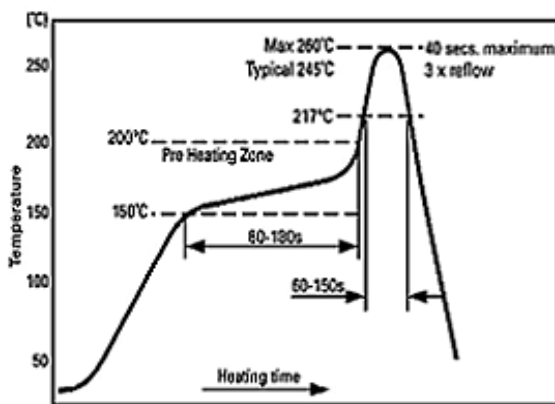
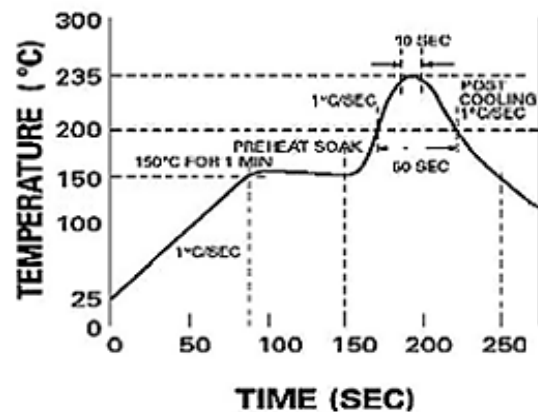


Figure 2



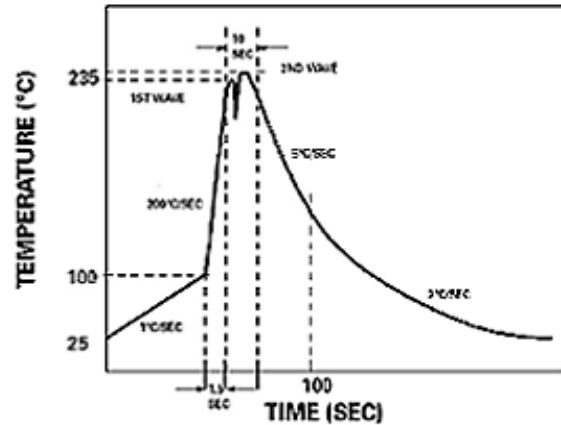
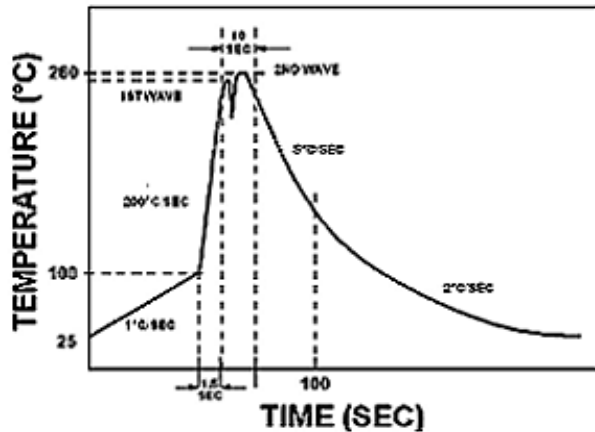
#### Reflow profiles in tabular form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~3°C/second	~3°C/second
<b>Preheat</b>		
– Temperature Range	150-170°C	150-200°C
– Time	60-180 seconds	60-180 seconds
Time maintained above:		
– Temperature	200°C	217°C
– Time	30-50 seconds	60-150 seconds
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	40 seconds
Ramp-Down Rate	3°C/second max.	6°C/second max.

### Recommended Wave Solder Profiles

The Recommended solder Profile For Devices with Pb-free terminal plating where a Pb-free solder is used

The Recommended solder Profile For Devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder



### Wave Profiles in Tabular Form

Profile Feature	Sn-Pb System	Pb-Free System
Average Ramp-Up Rate	~200°C/second	~200°C/second
Heating rate during preheat	Typical 1-2, Max 4°C/sec	Typical 1-2, Max 4°C/Sec
Final preheat Temperature	Within 125°C of Solder Temp	Within 125°C of Solder Temp
Peak Temperature	235°C	260°C max.
Time within +0 -5°C of actual Peak	10 seconds	10 seconds
Ramp-Down Rate	5°C/second max.	5°C/second max



### TYPICAL CHARACTERISTICS CURVE

Fig 1: Capacitance

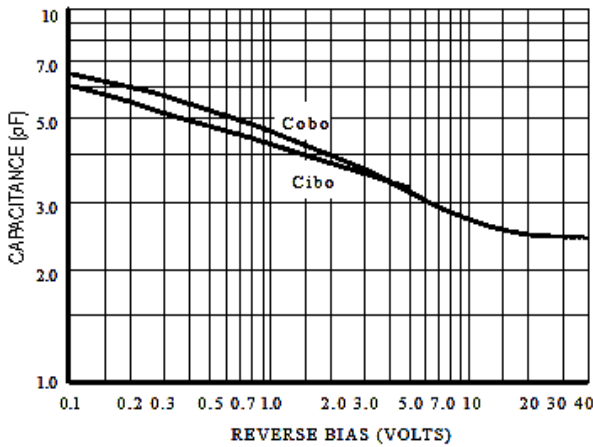


Fig 4: Charge Data

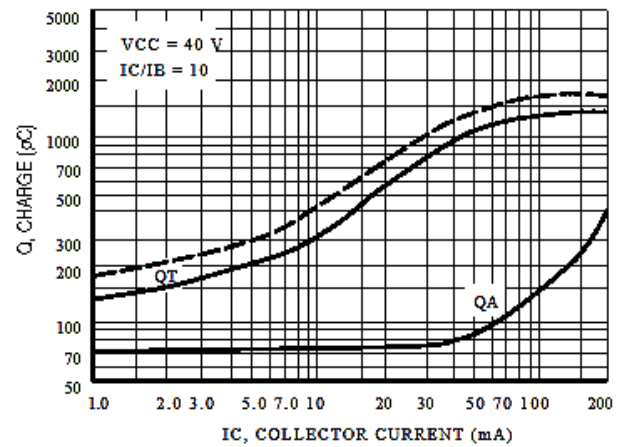


Fig 2: Turn On Time

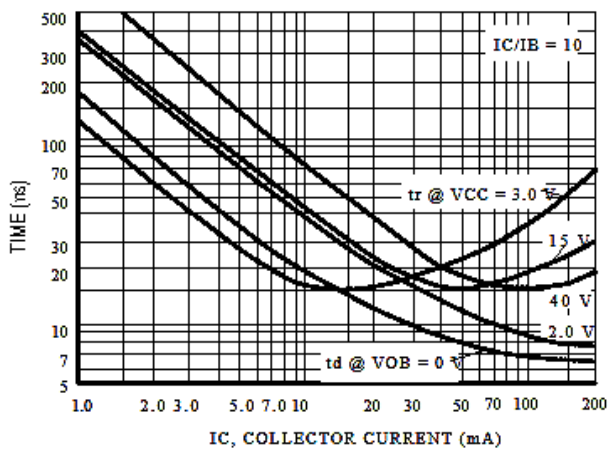


Fig 5: Fall Time

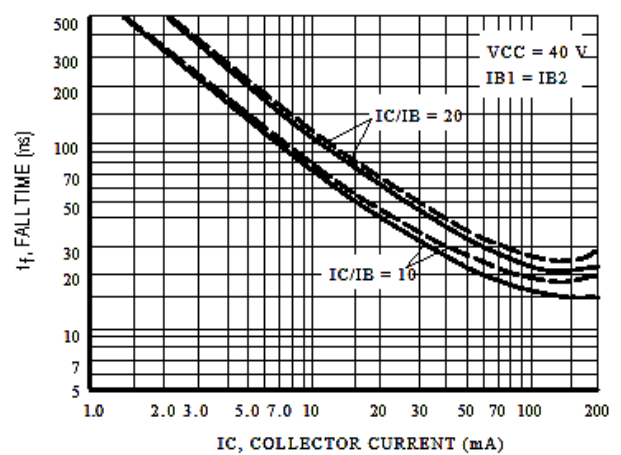


Fig 3: Noise Figure vs Frequency

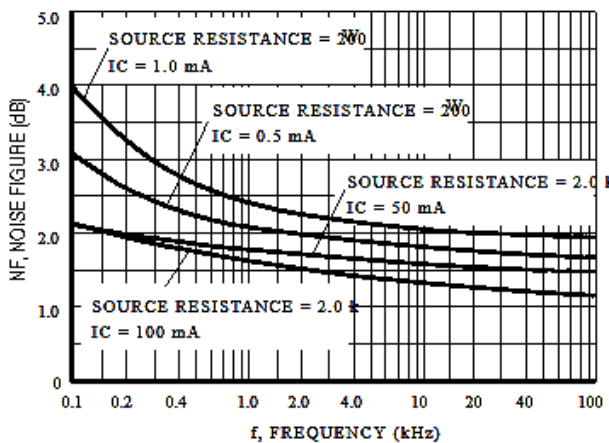
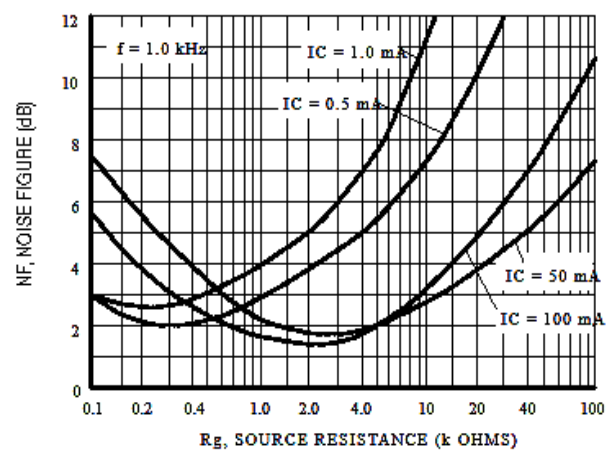


Fig 6: Noise Figure vs Source Resistance





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## TYPICAL CHARACTERISTICS CURVE

Fig 7: Current Gain

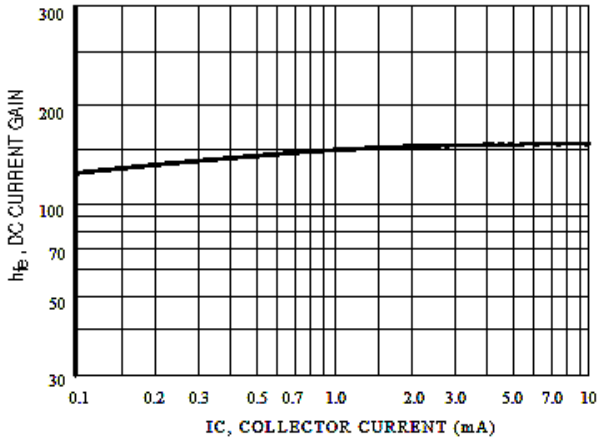


Fig 10: Output Admittance

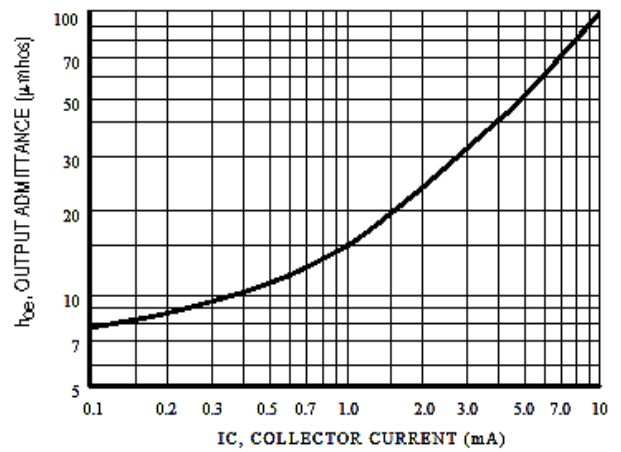


Fig 8: Input Impedance

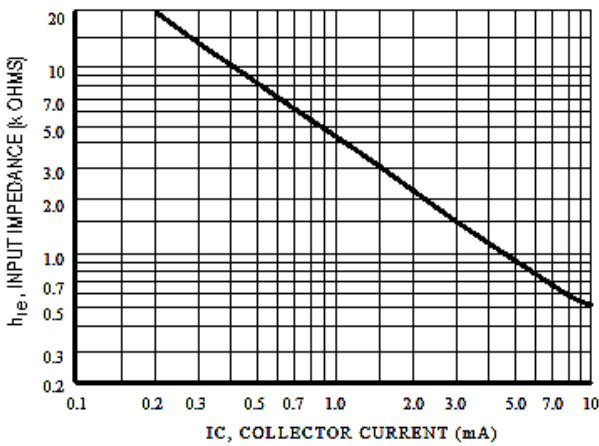


Fig 11: Voltage Feedback Ratio

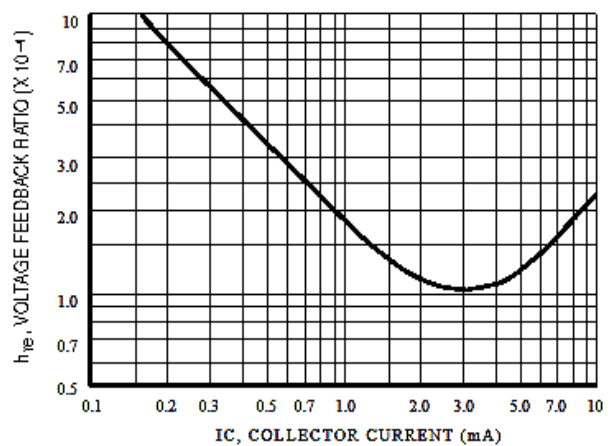


Fig 9: "On: Voltage

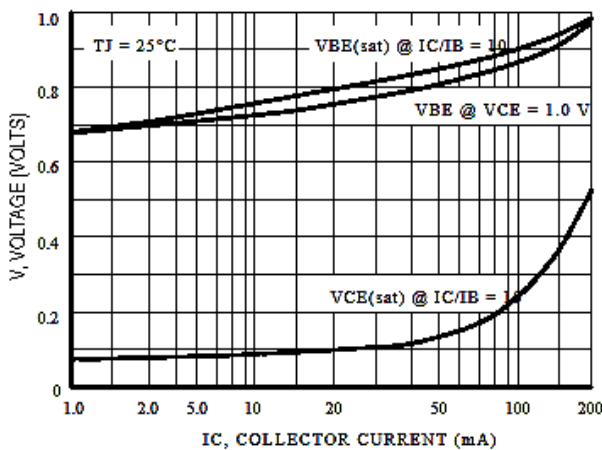
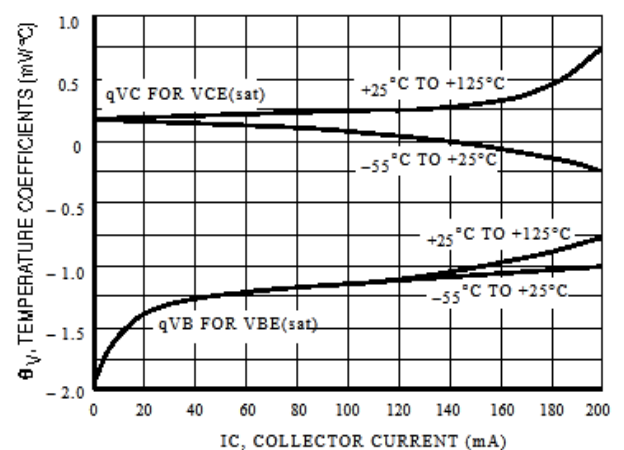


Fig 12: Temperature Coefficients



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## TYPICAL CHARACTERISTICS CURVE

Fig 13: DC Current Gain

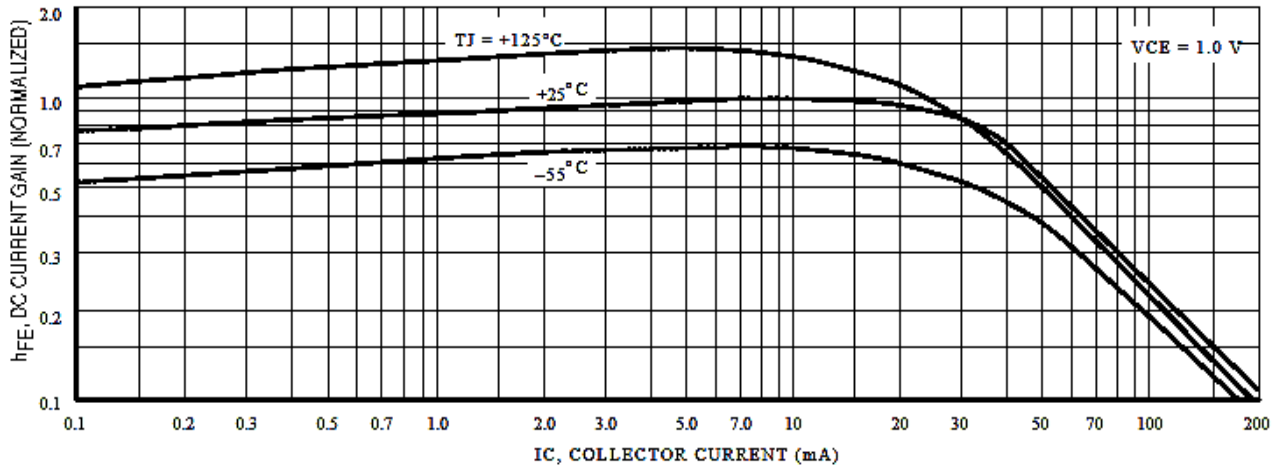
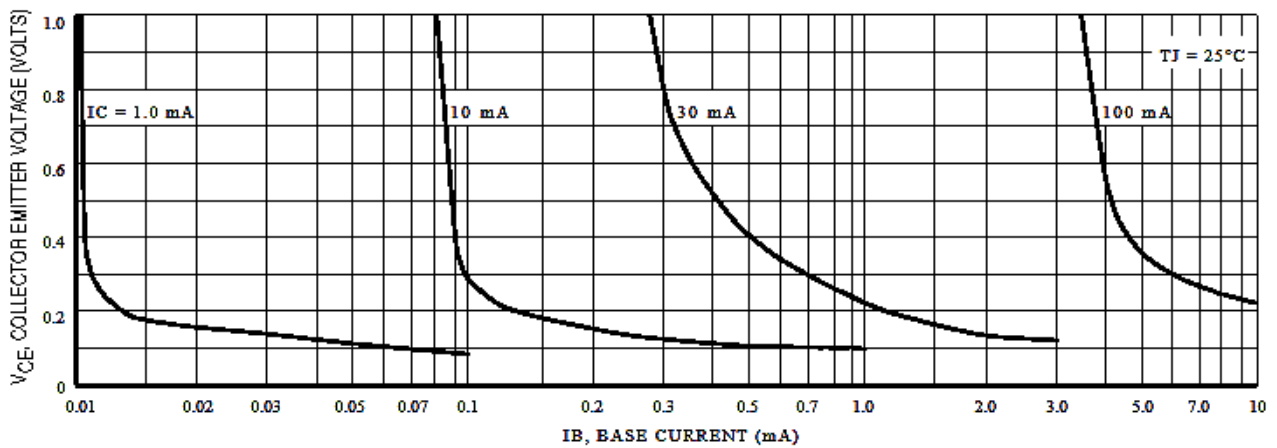


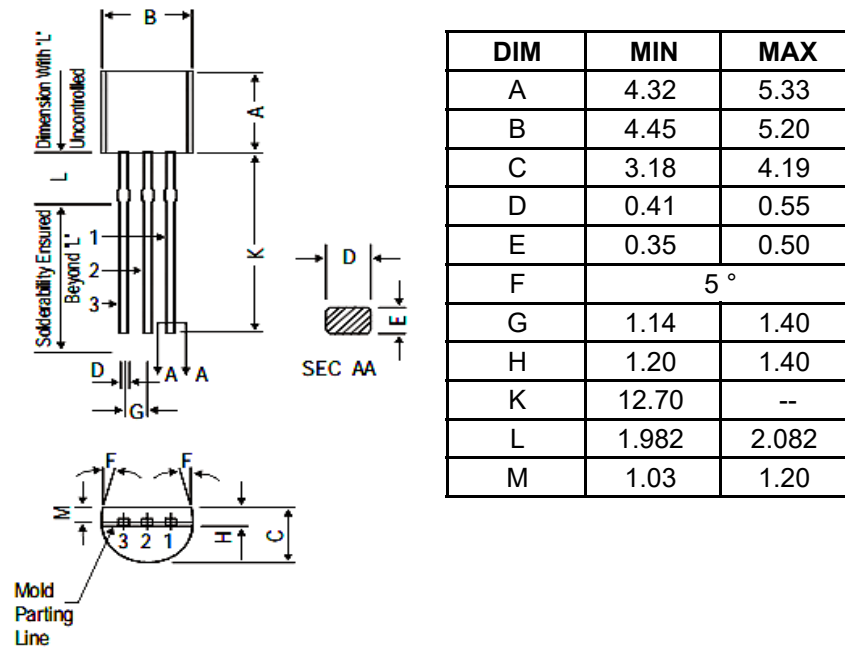
Fig 14: Collector Saturation Region



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## PACKAGE DETAILS

TO-92 Leaded Plastic Package



All Dimensions are in mm

## PIN CONFIGURATION

1. Collector
2. Base
3. Emitter

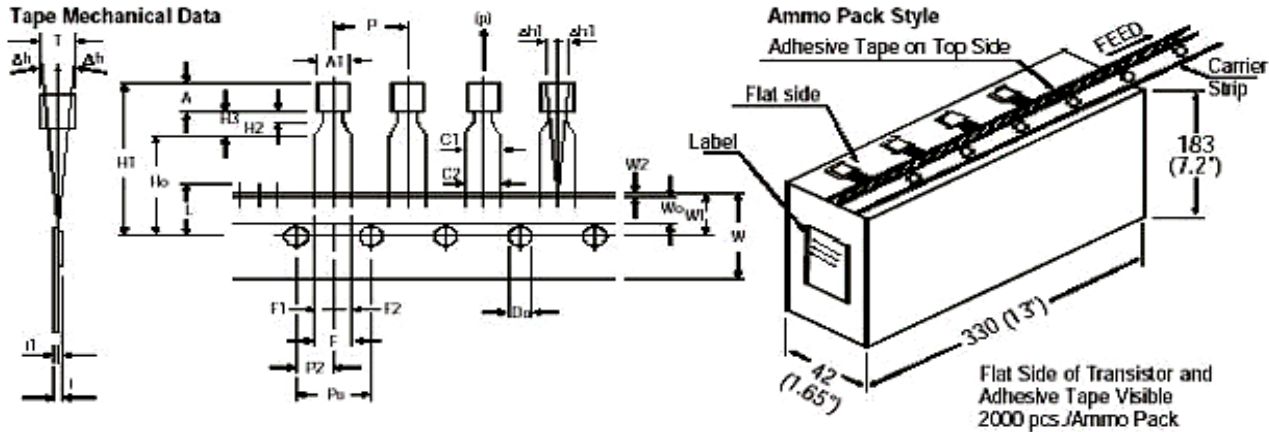


## Packing Details

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5K	17" x 15" x 13.5"	80K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2K	17" x 15" x 13.5"	32K	12.5 kgs



### TO-92 Tape & Ammo Pack



All Dimensions are in mm

ITEM	SYMBOL	SPECIFICATION			
		MIN.	NOM.	MAX.	TOL.
BODY WIDTH	A1	4.45		5.20	
BODY HEIGHT	A	4.32		5.33	
BODY THICKNESS	T	3.18		4.19	
PITCH OF COMPONENT	P		12.7		± 1.0
*1 FEED HOLE PITCH	Pe		12.7		± 0.3
*2 FEED HOLE CENTRE TO COMPONENT CENTRE	P2		6.35		± 0.4
DISTANCE BETWEEN OUTER LEADS	F		5.08		+ 0.6 - 0.2
*3 COMPONENT ALIGNMENT SIDE VIEW	$\Delta h$		0	1.0	
*4 COMPONENT ALIGNMENT FRONT VIEW	$\Delta h1$		0	1.3	
TAPE WIDTH	W		18		± 0.5
HOLD-DOWN TAPE WIDTH	W0		6		± 0.2
HOLE POSITION	W1		9		+ 0.7 - 0.5
HOLD-DOWN TAPE POSITION	W2	0.0		0.7	
LEAD WIRE CLINCH HEIGHT	Ho		16		± 0.5
COMPONENT HEIGHT	H1			24.0	
LENGTH OF SNIPPED LEADS	L			11.0	
FEED HOLE DIAMETER	Do		4		± 0.2
*5 TOTAL TAPE THICKNESS	t			1.2	
LEAD - TO - LEAD DISTANCE	F1, F2	2.40		2.70	- 0.1
STAND OFF	H2	0.45		1.45	
CLINCH HEIGHT	H3			3.0	
LEAD PARALLELISM	C1 - C2			0.22	
PULL - OUT FORCE	(p)	6N			

#### NOTES

- Maximum alignment deviation between leads will not to be greater than 0.2mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Holddown tape will not exceed beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
- There will be no more than three (3) consecutive missing components in a tape.
- A tape trailer, having at least three feed holes are provided after the last component in a tape.
- Splices should not interfere with the sprocket feed holes.

#### REMARKS

- \*1 Cumulative pitch error 1.0 mm/20 pitch
- \*2 To be measured at bottom of clinch
- \*3 At top of body
- \*4 At top of body
- \*5 t1 0.3 – 0.6 mm



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## Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

### Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be unconditionally shipped within this period. The period is defined as 2 years.

If products are stored longer than the shelf life of 2 years the products shall be subjected to quality check as per CDIL quality procedure.

The products are further warranted for another one year after the date of shipment subject to the above conditions in CDIL original packing.

### Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.

For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	Time	Condition
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH



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## Customer Notes

### Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

### Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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